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Modeling and performance analysis of advanced detection architectures for ADS-B signals in high interference environments

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Abstract

The RTCA DO-260B document has stimulated since a few years ago the adoption of novel algorithms to improve the ability of receivers to detect and decode ADS-B signals, with particular emphasis on preamble detection, declaration of bit state and confidence level, detection and correction of errors. Motivated by an industry-driven project, this paper reports on performance analysis of a set of enhanced techniques that we have developed for detection and decoding of ADS-B signals transmitted on 1090 MHz carrier frequency in high interference conditions. An extensive set of results has been derived through a specifically developed simulation environment, that is able to implement the features of both linear and logarithmic amplifier stages in the RF receiver architecture.

1 Introduction

Due to the continuous growth of air traffic and the requirement to increase the security levels, surveillance techniques for the provision of control services have assumed a key role, thus pushing for developing new methods of aircraft identification and tracking. The ADS-B (Automatic Dependent Surveillance - Broadcast) surveillance system fits these requirements, as its operation includes spontaneous and regular transmission of signals at 1090 MHz carrier frequency by aircrafts. The ADS-B system specifies the transmission (ADS-B 'out') and reception (ADS-B 'in') functionalities; by the year 2020 all existing aircrafts must be equipped with ADS-B 'out' to fly over European skies, while it is not yet mandatory to implement ADS-B 'in' [1]. The ADS-B signals transmitted on the 1090 MHz channel can suffer interference from signals generated by other systems that are operating on the same band, such as Secondary Surveillance Radar (SSR) replies. For this reason the RTCA guidelines [2] have been published to make more performing the algorithms nowadays used; furthermore new techniques have been also proposed to improve Extended Squitter (ES) reception in environments affected by high interference [3], [4], [5]. In the above framework this paper focuses on the overlapping issue of unwanted replies on Mode S/ES signals. Specifically, we present enhanced receiving techniques in the presence of interfering signals and evaluate the performance in correct detection and decoding of ADS-B signals. The performance analysis is reported for two different alternatives of RF receiver chain: logarithmic and linear models. The whole transmission and processing stages have been implemented in a detailed simulation framework.

2 Enhanced reception techniques for ES

The ES frame is 120 μs long, with the 120 bits allotted in 8 bits of preamble and 112 bits of data block encoded with Pulse Position Modulation (PPM) [6]. The preamble

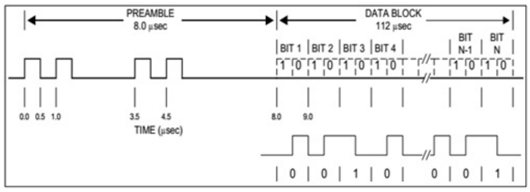

Figure 1. ADS-B frame structure

is formed of four pulses in fixed positions within an 8 μs time interval, which allows synchronization on the receiving side. The first step of the reception process is the acknowledgment of the message start through the identification of four pulses in a specific position, as established by the standards; the next step concerns the data block decoding, which also implements the error detection and correction processes.

The preamble detection is the most complex step of the entire process and includes pulse labeling (Valid/Leading), feasible preamble recognition and power reference level calculation. A set of tests is applied to pulses of each detected preamble for the validation, that include the verification of possible signal overlapping in standard positions, the verification of consistency of power levels and the presence check of at least one pulse in each DF (the first five bits) field bits. The preamble detection phase is able to identify different preambles per frame interval, but the decoding process can only elaborate a signal at a time if we use a single receiver chain. To comply with this limitation, the retriggering function has been introduced in our system: therefore, we discard preambles in our processing chain whenever a possible preamble with larger reference power level is detected.

For the decoding phase three different techniques have been implemented: Central Sample (CS), Advanced Central Sample (ACS), Multi-Sample (MS). The CS technique is based on the comparison between the amplitudes of central samples of the two chips composing each bit and involves the use of a reference threshold for determining the confidence level associated to the decision. The ACS technique introduces a power range to model the logic state, with the confidence level that depends on how the two chips fall into the range. The MS technique involves the use of multiple samples for the single chip, a range for checking the appropriateness of power levels and a threshold for discriminating the low power regime; furthermore, it uses more complex computation algorithms.

Conservative techniques for error detection/correction have been considered. These techniques, as well as the detection techniques, have been implemented taking into account the RTCA guidelines; nevertheless, we have taken into account the realistic dynamics of signals produced by the transmitter block and in accordance with the sampling frequency (24 MHz) to be actually used in the target platform.

3 Simulation model of advanced transceiver chains for ADS-B signals

General Simulation Model

The general model of the system provides two main functional blocks associated to transmission and reception of ADS-B signals; the second one implements the advanced algorithms briefly presented in the previous section. The

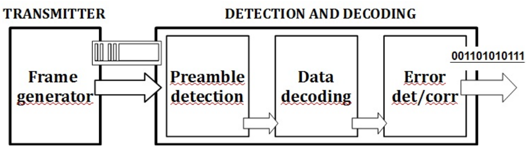

Figure 2. Simulation Model

transmission block incorporates the frame generation phase and a detailed model of the analog section of a real reception chain; it also includes the D/A conversion that returns the Extended Squitter baseband signal. The generated signal, which is then distorted and disturbed by noise and by the presence of Mode A/C replies and other ADS-B frames, is provided as an input to the reception block. In particular, the frames are modeled taking into account the internal structures of both linear and logarithmic reception chains. The Frame generator block provides three different types of signal: Primary and Secondary ADS-B frames, and Mode A/C replies. Each signal generation function has a specific configuration about temporization and power levels. All pulses are generated at 60 MHz intermediate frequency with reference to the standard frame structure, before being moved into the specific RF receiver chains; for Extended Squitter signals a tolerance on carrier frequency of ± 1 MHz has been introduced, as well as a random phase shift for each generation of Mode A/C replies.

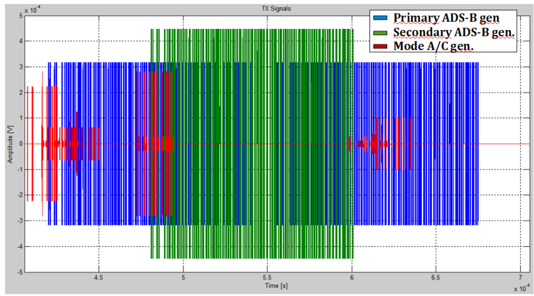

Figure 3. Signal generation

Logarithmic and Linear ADS-B receivers

The combination of signals generated by the various sources is taken as the input to the block that models either Logarithmic or Linear receivers (receiver type can be selected on the setting window). Finally we include the functional diagrams of receivers that implement the advanced detection algorithms and the blocks that support the definition of operating scenarios, with particular interest for high traffic conditions (e.g. 40000 FRUIT/s).

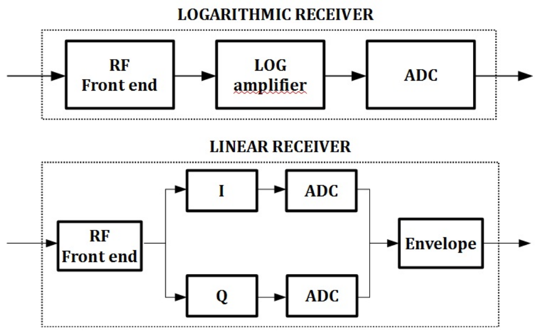

Figure 4. RF receiver models

Logarithmic receiver: the equivalent model of the system is developed as in the diagram of Figure 4 according to three main blocks: RF front end, amplifier block and ADC. The RF reception block includes a first amplification stage, that takes the signal from the antenna block as the input, and sups up the equivalent thermal noise introduced by that portion of the receiving chain. The logarithmic amplifier is then modeled through the implementation of the characteristic function of the real component and the related component of thermal noise. The quantization process is implemented taking into account the rounding law and a uniform model for quantization of the reference range into 1024 intervals (10-bit encoding).

Linear receiver: the receiver model is structured in the cascade of two main macro blocks: a RF processing block identical to the previous case and a two-lines phase-quadrature receiver, which implements the generation of in-phase and quadrature harmonic signals at 60 MHz frequency (with tolerance of ± 50 KHz), low-pass filtering and AD conversion with 16 bit encoding on both lines, and envelope calculation. In Figure 5 an example is shown where the responses of the two RF receiving blocks to the same stimulus are plotted; the result signal is the test signal to be sent as the input to the detection/decoding system.

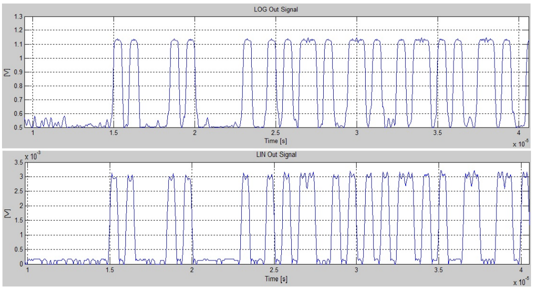

Figure 5. Output signals from the RF receiver.

4 Simulations and Performance Results

An extensive set of tests have been run for comparative performance evaluation of the advanced detection algorithms in the presence of both linear and logarithmic receiver models. In this frame we have also paid attention to the related hardware implementation perspectives.

When considering the preamble detection, the eligible thresholds for input dynamics have been determined and specific cases have been addressed for quantifying the failures in detection due to noise and interference; when considering decision alternatives on traffic data, results are reported in terms of BER (Bit Error Rate).

For the definition of the input range (MTL threshold, we refer to simulation tests in the presence of thermal noise only. Strong interference (40000 FRUIT per second = 5 FRUIT on average for the ADS-B frame interval)has been instead considered when evaluating the performance of decision techniques.

Preamble detection results
Figure 6 shows simulation results about preamble detection. Specifically for the definition of MTL threshold in the case of logarithmic reception we consider simulation runs where ADS-B frames are only disturbed by noise in the environment associated to the RF receiver chain and by noise introduced by logarithmic amplification process; in the case of linear reception we will consider only the RF noise. In the figure the Sp parameter denotes the signal power related to the real signal from the antenna output. By observing that the maximum level for input signal is -15 dBm, it can be affirmed that the dynamics of the logarithmic receiver to be considered for the detection algorithms of interest is about 70 dB; instead the dynamics is reduced by about 8 dB when the linear receiver chain is considered. The presence of interfering signals (FRUIT) can impair the preamble detection process; at low power levels (<-70 dBm) the effect of noise is relevant, with consequent increase of the MTL threshold and degradation of performance when mode A/C replies overlap. Below we discuss three cases of overlapping of Mode A/C replies that produce the failure of preamble detection process and data decoding:

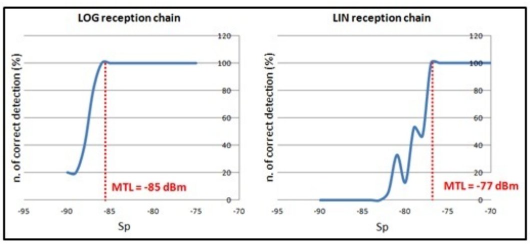

Figure 6. Performance results for preamble detection

1) *Direct interference on the preamble pulses*: Figure 7 depicts the case with direct interference of the FRUIT on one of the preamble pulses, specifically on the last pulse. The destructive combination causes masking of the

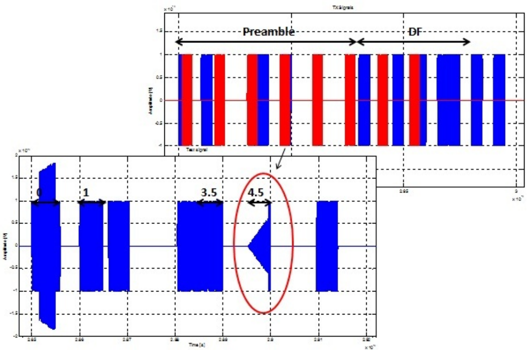

Figure 7. Leading Edge/Valid Pulse masking

Leading / Valid edge in 4.5 ms position. Therefore the pre-detection process fails and the useful preamble is not detected. There is no way to avoid this situation because the frame is distorted in its essential references of the preamble.

2) *Detection of a false preamble that precedes the one really transmitted*: the detection and validation of the false preamble implies that the data block associated with it is brought at decoding. In this case, which is shown in

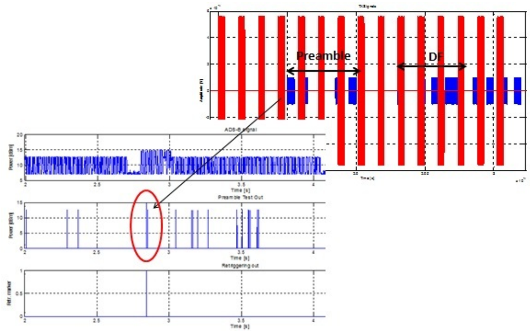

Figure 8. False preamble detection

Figure 8, the reference power of the preamble actually transmitted is smaller than the signal being processed; the retriggering algorithm can not recover this situation and

the actual frame is discarded.
3) *Incorrect calculation of reference power level*: this situation usually occurs whenever the FRUIT overlaps in correspondence of the beginning of the preamble pulse. In

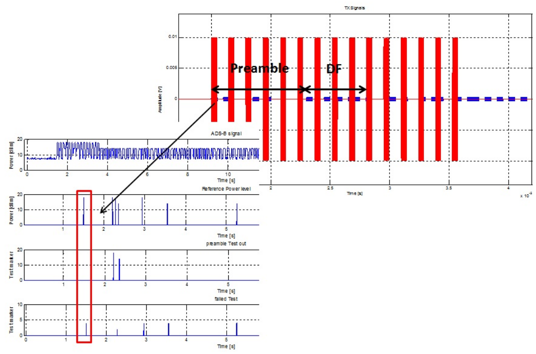

Figure 9. Error on the reference power level calculation

the example shown in Figure 9 the presence of a FRUIT does not change the state of the Leading Edge associated with the first pulse sample; the next samples, although corrupted, are taken into consideration for calculating the reference power. The result is not consistent with the power level of the five DF pulses, therefore the DF validation test will succeed with consequent rejection of the preamble.

Decoding results
The following results, that refer to the advanced decision techniques previously described, have been obtained from simulations carried out with an interference level determined by 40000 FRUIT per second. Specifically the results have been obtained with both RF receiver chain alternatives, random FRUIT power level in the range [-90 dBm, -15 dBm], and ADS-B frame power level which was let to vary from -90 dBm to -15 dBm.

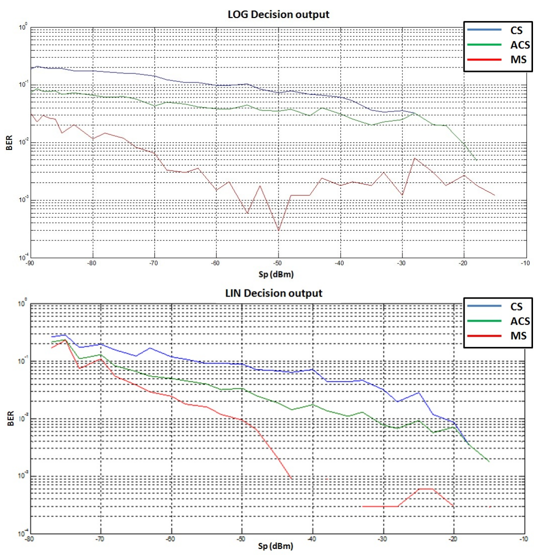

Figure 10. Simulation results on decoding techniques

5 Concluding Remarks

From inspection of performance results obtained in terms of BER for the advanced decoding techniques, we observe that the MS alternative can substantially return a very low BER level even in very situations affected by high FRUIT interference. In particular, the MS technique works very well when strong overlaps occur, while it presents some limitations when overlapping signals have larger power: in this case the ACS seems more suitable. The same preamble structure was developed to combat individual Mode A/C replies interferences, and the whole enhanced detection chain has also provided good performance in the selection of the most reliable preambles with high FRUIT interference. When the RF receiver model is concerned, the logarithmic receiver seems to outperform the linear receiver in the lower power regime; on the contrary, the performance gap is negligible when medium-large power levels are concerned.

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