On-Chip Microstrip Patch Reflectarray

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Abstract

This paper investigates the radiation characteristics of on-chip microstrip patch reflectarray for 60 GHz system. The proposed reflectarray is fed using on-chip cylindrical dielectric resonator antenna, CDRA placed at a distance 42.5 mm from the array aperture. The antenna introduces good impedance matching at 61 GHz. The impedance bandwidth is 1.35 GHz. The reflectarray consists of 289 unit-cell elements covering an area of 42.5 x 42.5 mm² in x-y plane. Each unit-cell element consists of a square microstrip patch surrounded by four rectangular strips. The phase of the reflected plane wave from the unit-cell element is controlled by varying the patch length. The reflectarray structure and the CDRA are simulated using full wave simulation, finite integration technique, FIT. A maximum gain if 17.5 dBi is achieved and 2.85 % bandwidth is obtained. Offset beams scanning in different directions are investigated.

1. Introduction

Recently, much attention has been drawn for high data rate wireless communication systems at 60 GHz unlicensed bands [1]. Network on chip (NoC) is a communication subsystem on an integrated circuit (chip), between multiple cores on the communication system. Generally, most ICs have been designed with defined connections for each signal. Large systems designs have several limitations in the wire interconnection design. The wires occupy much of the area of the chip, increase the delay, and increase the power dissipation as the signals propagate through them. Wireless chip-to-chip data communication can be a solution of this problem. The requirements for antenna design for chip wireless interconnection are low cost, high radiation efficiency and easy integration with other components. The complementary metal-oxide semiconductor (CMOS) ICs introduces a valuable technology for system on chip applications [2]. Recently, different CMOS on-chip antennas have been introduced to fulfil the demands of the 60-GHz system [3]. A microstrip patch array with cooperative feeding network for 60 GHz packaging has been investigated in [4]. The on-chip microstrip antenna suffers from narrow bandwidth and increases losses in the feeding network. The dielectric resonator antennas (DRAs), operating on microwave and millimeter wave band for on-chip communications, have been investigated in [5]. DRAs offer many advantages such as compact size, large bandwidth, and high radiation efficiency. Low-cost, low-profile, high gain reflectarrays are antennas have been used since 1960 [6]. The Constituent elements of the reflectarray that are set into a regular arrangement imitate the function of the phased array radiating elements. A basic reflectarray collimates waves from a feeding antenna into a directive beam by applying a phase correction to the reflected field from each unit-cell element on the reflectarray surface by changing the characteristics of the individual elements. Reflectarrays use the free space medium as a transmission medium to transfer signal from the feed to the elements and thus avoid degradation in the gain performance as a result of loss in the feeding networks. A 0.25 µm Bi-CMOS system-on-chip with four transceivers for Ka-band active reflectarray have been introduced in [7].

In this paper, the radiation characteristics of 17×17 on-chip microstrip patch reflectarray fed by on-chip DRA for 61 GHz applications have been proposed. The design of the reflectarray and the DRA feeder takes into account the required multlayer structure needed for the chip integration. The paper is organized as follows: Section (3) introduced the design for the proposed unit-cell element and its reflection characteristics. Section (4) demonstrates the design steps of the reflectarray, feeding element and their radiation characteristics. Finally, Section (5) concludes the main results demonstrated through the paper.

2. Design of unit-cell element

The detailed structure of on-chip microstrip unit-cell element for 60 GHz chip-to-chip communications is shown in Fig. 1a. The unit-cell element consists of conductor square patch with arm length, Lp, surrounded by four rectangular strips with length, Lp, width w=Lp/12, and separation g=0.09 mm. The patch is printed on a square silicon oxide substrate with dielectric constant ε=4, arm length Lc=2. 5 mm and thickness hs=225 µm is placed below the silicon oxide layer. A perfect electric conductor, PEC, ground plane is placed on the backside of the unit-cell element. The microstrip patch length, Lp, is varied to control the reflection coefficient of the structure at 61 GHz. The variations of the reflection coefficient, magnitude and phase, versus the patch length, Lp, are determined using the FIT technique [8] at 61 GHz as shown in Fig. 1b. The reflection coefficient phase variation is calculated by analyzing a periodic array of
identical unit-cell elements illuminated by a normal incidence plane wave. Reflection coefficient magnitude from 0 dB to -0.15 dB and 342° phase variations for \( L_p \) varied from 0.34 mm to 0.82 mm are obtained.

Figure 1. a. The structure of the microstrip patch unit cell with perfect conductor ground plane, b. The variation of reflection coefficient phase and magnitude versus the patch length \( L_p \) of the patch unit-cell at 61 GHz.

3. Design of 17×17 on-chip microstrip patch reflectarray

Figure 2 introduces the layout of 17×17 on-chip microstrip patch reflectarray in x-y plane. The phase compensation, \( \phi_{ij} \), required to focus the reflected waves into plane waves with designed deflection angles \( (\theta_d, \phi_d) \), is calculated, as follows [9]:

\[
\phi_{ij}(x_{ij}, y_{ij}) = k_0 (d_y - \sin \theta_d (x_{ij} \cos \phi_d + y_{ij} \sin \phi_d))
\]

\[
d_y = \sqrt{(x_y - x_f)^2 + (y_y - y_f)^2 + (z_f)^2}
\]

where \((x_{ij}, y_{ij})\) is the position coordinates of each element in the array structure, and the feed is located at \((x_f, y_f, z_f)\). The computations are based on a full-wave analysis of the problem and are taking into consideration the effect of the mutual coupling between the elements using the FIT. The reflectarray is fed by on-chip CDRA placed at distance 42.5 mm from the array apertures as shown in Fig. 3. The CDRA has a radius \( R_d = 0.355 \) mm, height \( H = 0.325 \) mm and dielectric constant \( \varepsilon_r = 48 \). The CDRA is fed by microstrip transmission line with \( W_f = 0.08 \) mm and \( L_f = 0.83 \) mm printed on silicon oxide substrate with thickness \( h_o = 0.01 \) mm. Silicon substrate is set below the SiO\(_2\) layer with thickness \( h_s = 0.225 \) mm. The on-chip CDRA dimensions are optimized to resonate at 61 GHz. The variations of the reflection coefficient and the input impedance versus frequency for the on-chip CDRA are shown in Fig. 4. The results are calculated using finite integration technique and compared with that calculated by the finite element method. Good agreement between the two methods is obtained. The input impedance is \( 44 + j3 \) \( \Omega \) at 61 GHz. The antenna introduces good impedance matching at 61 GHz with -10 dB impedance bandwidth of 1.35 GHz (from 60.1 GHz to 61.45 GHz). The antenna gain variation versus frequency at the boresight direction is presented in Fig. 5. The CDRA introduced peak gain of 5.6 dBi with variation of ±0.5 dBi over the entire band (from 54 GHz to 66 GHz). The E- and H-plane radiation patterns for the on-chip CDRA at 61 GHz are shown in Fig. 6. The CDRA introduces broad-beam with half power beamwidth, HPBW of 113 and 104 degrees in E- and H-plane, respectively. The complete array structure including the 17×17 on-chip microstrip patch reflectarray and the on-chip CDRA are simulated using the FIT. The computed radiation patterns of the microstrip patch reflectarray in E-plane and H-plane at 61 GHz are shown in Fig. 7.
Figure 3. The structure of on-chip Cylindrical Dielectric Resonator Antenna with $L_s = 2$ mm, $h_s = 0.225$ mm, $h_o = 0.01$ mm, $L_f = 0.83$ mm, $W_f = 0.08$ mm, $R_d = 0.355$ mm, $H = 0.325$ mm.

Figure 4. The variations of the reflection coefficient and the input impedance versus frequency for the on-chip DRA.

Figure 5. The variation of the gain versus frequency for the on-chip DRA at the boresight direction.

Figure 6. The E- and H-plane radiation patterns for the on-chip DRA at 61 GHz.

Figure 7. The E- and H-plane radiation patterns versus elevation angle for microstrip patch reflectarray at 61 GHz.

Symmetrical gain patterns are obtained due to the symmetry of the array. The first side lobe level, SLL, relative to the main lobe is 14.2 dB in the E-plane compared to 10.5 dB in the H-plane. The response of reflectarray gain against frequency at the boresight direction is shown in Fig.8. A maximum gain of 17.5 dBi was achieved. A 2.85% bandwidth (1.7 GHz) with 1-dB gain variations was
depicted. The reflectarray has an inherent narrow bandwidth, because of the nature of the microstrip patch unit-cell element. The radiation in the back direction is due to the diffracted field from the finite area of the array or the edges of the array as well as the spillover which takes place all around the array in the back region. To provide communication links in different directions between the on-chip circuits and avoid blocking and interference between the different communication links, the reflectarray is designed to give offset beams at different deflection angles by assigning the appropriate phases for the radiating elements within the reflectarray at different deflection angles: 15°, 30°, and 45°. Figure 9 indicates the gain pattern versus the elevation angle of the microstrip patch reflectarray at 61 GHz and φ=0° for scanning from -45° to +45°. As the scanning angle is increased the gain is decreased. The side lobe level increases as the angle of the beam increases.

Figure 8. The variation of reflectarray gain against the frequency at the boresight direction.

Figure 9. The gain versus elevation angle for the microstrip patch reflectarray at 61 GHz with offset beams at directions θ=±15°, ±30° and θ=±45° and φ=0°.

4. Conclusions

This paper introduces a design of 17×17 on-chip microstrip patch reflectarray fed by on-chip CDRA for 61 GHz chip-to-chip communications. The proposed unit-cell element consists of a square microstrip patch surrounded by four rectangular strips printed on silicon oxide and silicon substrates backed by a PEC ground plane. The unit-cell element introduces a reflection coefficient magnitude from 0 dB to -0.15 dB and 342° phase variations for the patch length varied from 0.34 mm to 0.82 mm. The on-chip DRA impedance matching bandwidth is 1.35 GHz with peak gain of 5.6 dBi. The CDRA is used to feed the reflectarray. The radiation characteristics of the 17×17 on-chip microstrip patch reflectarray are simulated using the FIT. A maximum gain of 17.5 dBi with 2.85% 1-dB gain bandwidth was depicted. Design of microstrip patch reflectarrays for beam scanning in different directions are investigated. The proposed on-chip reflectarray introduces a good candidate for wireless interconnection between electronic components.

5. References