

A High Precision Signal Analysis System Based on SoC

Bin Li, Jiayun Song, Mingzhi Zhang
Beijing Oriental Institute of Measurement and Test

Abstract

This paper describes a high precision signal analysis system of SoC, which can accurately measure the signal amplitude, frequency, and other parameter. The FFT can analyze the amplitude of the signal after ADC collecting and windowing the data, and the Equal-precision frequency measurement model could accurately measure the signal. The signal analysis system depended on the method works accurately, stably, and high integrity, with a wide application.

1. Introduction

The precision measurement of real signal has been studied by the experts in many fields. Usually, AC signal measurements are measured after the AC-DC conversion, as the accuracy of AC-DC conversion runs into the bottleneck, more methods have been developed.

With the rapid development of computer science and chip manufacturing technology, data acquiring, processing and transmitting have been developed in the direction of high precision, small volume, and high throughput. So, people can more accurately understand, analyze, and recognize signals. In some situations, which need high precision measurement and low-power dissipation, the Xilinx SoC (System on a Chip) can complete the task more efficiently, the FPGA frequency can run above 250M stably, drive the ADC (Analog to digital converter) then obtain digital data efficiently. At last, through FFT (Fourier transforms) and other algorithms, we can analyze the various signal parameters, accomplish the functions of frequency and amplitude measurement as well as the results display with the ARM core chip.

2. Key principle

2.1 Equal-precision frequency measurement

In this paper, we are using the equal-precision measurement method, equal-precision frequency measurement method is based on the development of direct frequency measurement method, and its actual gate time is not fixed, but the measured signal cycle integer times, it is synchronized with the measured signal, so called multi-periodic synchronization method. This method achieved that the rising edge of N_x synchronize with the rising edge of N_s , and because of that, it eliminated the error and improved measuring precision, it also achieved equal-precision frequency measuring during all measure period. The principle of frequency measuring and waveforms are as follows:

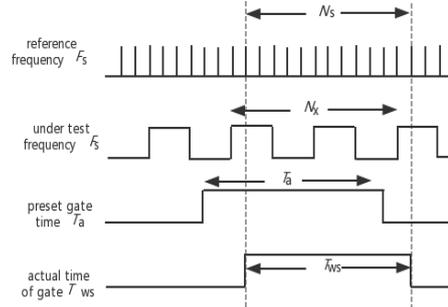


Figure 1. Equal-precision frequency measurement principle block diagram

Let us suppose the frequency of standard signal is F_s , and the frequency of measured signal is F_x , the counter of measured signal is N_x while the measuring period T_{ws} . The counter of standard signal is N_s , so we can conclusion the formula: $\frac{N_s}{F_s} = \frac{N_x}{F_x}$, in the measurement process, there are two counters on the standard frequency signal F_s and the measured frequency signal F_x . Then the two counters do not start counting until the rising edge of the measured frequency signal comes, the two counters really start counting. Then when the preset gate falling edge of the closure signal comes, the two counters do not immediately stop counting until the rising edge of the measured frequency signal to stop counting, the completion of a measurement process. From the above equation, we can see the frequency of the measured signal is related to the frequency of the signal, and increased the measurement period T_{ws} , F_s or N_s , we can reduce the relative error and improve the measurement accuracy.

Measurement accuracy, the actual gate time and standard signal frequency is related to F_s , and independent of the signal frequency to measuring, therefore we can obtain a high precision result.

2.2 FFT

In Fast Fourier transform, the N-point DFT of a sequence X_n is defined as follows:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}$$

in this formula, $k=0 \cdots (N-1)$, $W_N^{nk} = e^{-j2\pi/N}$ was called twiddle factor, calculating an N-point complex sequence X_k of the DFT requires N^2 and $N \times (N - 1)$ complex additions. Therefore, when N is large enough, the amount of N-point DFT calculation is very slow. FFT algorithms proposed in 1965 by Cooley-Tukey, he used the periodicity and symmetry of W_n , made the length of DFT into smaller points, such computational complexity from N, reduced to $N \log_2(N)$, thus greatly reduced the workload, improved the operation speed.

The Fastest Fourier Transform in the West (FFTW) is a software library for computing discrete Fourier transforms (DFTs) developed by Matteo Frigo and Steven G. Johnson at the Massachusetts Institute of Technology [2]. It is possible to efficiently carry out a Discrete Fourier Transform(DFT) of arbitrary dimensions, Discrete Sine Transform (DST) and Discrete Cosine Transform (DCT), and it is the most effective transformation tool at now. It can automatically adjust the algorithms parameters accorded to the users' underlying hardware properties to get the best solution, such as cache, memory, register size and so on. The new edition library also supports shared storage multithreaded parallel and distributed storage MPI (Message Passing) in parallel.

2.3 Window

The windows truncate the continuous signal and then we can use the FFT algorithms to get the signal spectrum, amplitude and other paramant. Different windows obtain different amplitude spectrum precision, this paper present the most widely Flat Top window function to analyze and calculate the amplitude spectrum of the window function of the form is

$$\omega_j = \sum_{k=0}^m c_k \cos\left(k \times \frac{2\pi j}{N}\right)$$

In the formula, $j=0 \dots (N-1)$, c_k for the constant of k , N for the FFT calculation points,

$$\omega_j = 1 - 1.985844164102\cos(z) + 1.71176438506\cos(2z) - 1.282075284005\cos(3z) + 0.667777530266\cos(4z) - 0.240160796576\cos(5z) + 0.056656381764\cos(6z) - 0.008134974479\cos(7z) + 0.000624544650\cos(8z) - 0.000019808998\cos(9z) + 0.000000132974\cos(10z).$$

3. Implement

3.1 The overall program design

The SoC technology has greatly improved the performance of single-chip, at the same time, the degree of integration is greatly increased, making it possible to miniaturize high performance devices. The following figure shows the block diagram SoC system.

ADC driver actuates the ADC converting the analog signal to digital data, frequency driver actuates the frequency measurement model converting the frequency of signal to digital data. All the data are accessed through AXI4, AXI-Lite to Linux system operation on the ARM core, these data buses through the entity into a Linux character device, by reading or writing these devices can communicate with FPGA. The application reading the device data, windowing the signal, do FFT calculating by Multi-Core, Multi-threaded tec. At the same time, the built-in TCP server can communicate with other remote clients, Signal amplitude, frequency, waveform interact with user by UI, at the same times, we can communicate with peripheral circuit through SPI, USART.

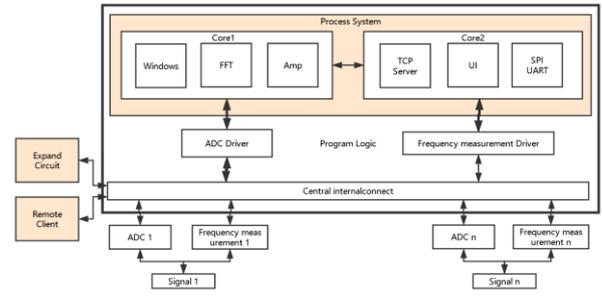


Figure 2. Total frameworks

3.2 System software design

Figure 3 shows the system software flow chart, after the system powered on, FPGA was initiated, the central internal connect initiated frequency measurement module and configured ADC driver, then started the Linux system, at last, the application started automatically during the system booting. App initialized TCP server threads, read device thread, FFT thread, UI thread, peripheral threads.

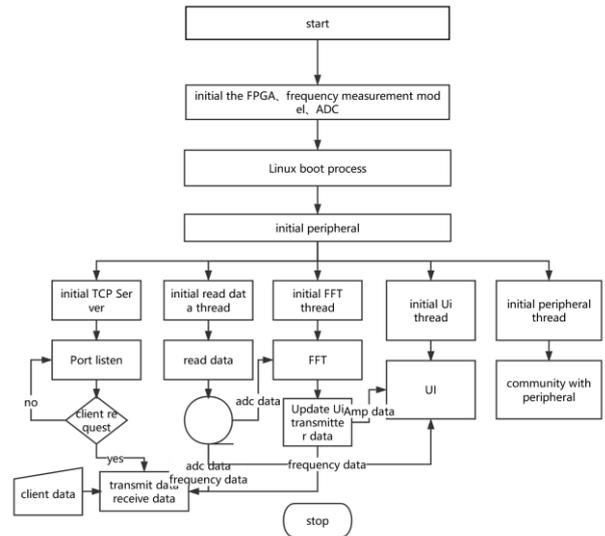


Figure 3. System software flow

3.3.1 Frequency measurement

Equal-precision measurement process will produce two result, N_x and N_s , both are 32-bit, but the AXI4_Lite is 8-bit width only, these interfaces must use a dual-port RAM, this method can achieve the data transmission, but it is difficult to read the measurement data once in the real time, prone to errors. Therefore, the effective implementation block diagram and flow as follows:

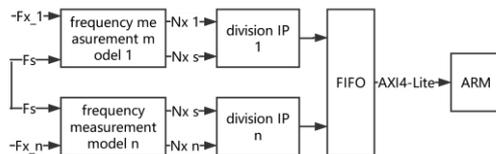


Figure 4. Frequency measurement software flow chart

3.3.2 Amplitude measurement

The FPGA can analyze the data which obtained by ADC, and it can be analyze by the ARM core, which

depend on the data size or application complexity. this paper selected the latter method. FPGA data transfer to the Linux character device by AXI bus, the application read device and restructure each channel data and sent to the windowing thread, FFT thread to analyze. Specifically use FLAT-TOP window, select a different calculation to obtain a different number of points depending on the accuracy and precision requirements of the measuring range, the accuracy of the analysis results. FFT spectrum as CORDIC algorithm data source, you can get the signal amplitude, angle, and other information. FFT calculation Process as shown below

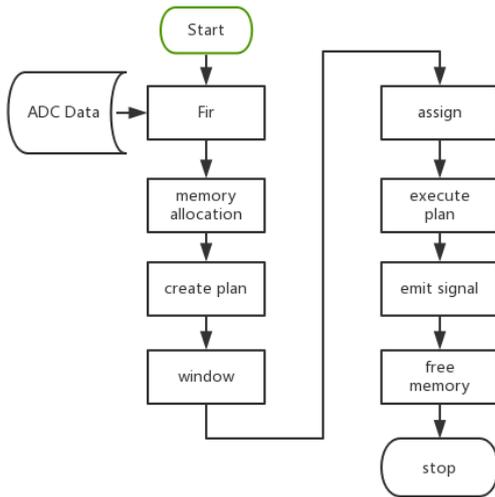


Figure 5. FFT calculation process

4. Experiment data

4.1 Frequency measurement

The test system: function generator Agilent 33522A, frequency meter Agilent 53131A, digital multimeter Agilent 34401A. Frequency measurement results shown below, the measured frequency of 1000Hz, the crystal frequency is 100MHz, the crystal frequency stability of 25ppm, frequency crystal preheated correction value 1000.00169 results correction value.

$$f_x = \frac{N_x \times F_s}{N_s} = \frac{1000 \times 100000169}{100000154} = 1000.00015$$

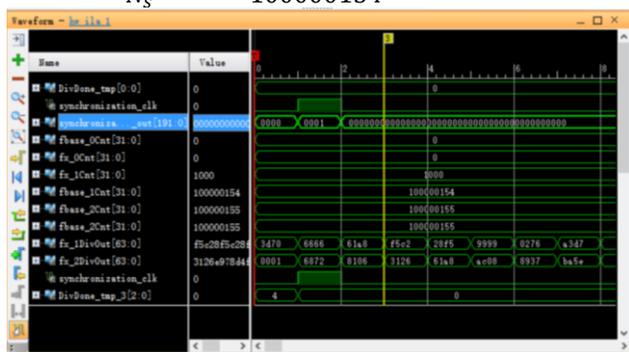


Figure 6. frequency measurement debug result

Figure 7 shows the relative error of frequency measurement, the relative frequency measurement error is 2.0×10^{-7} .

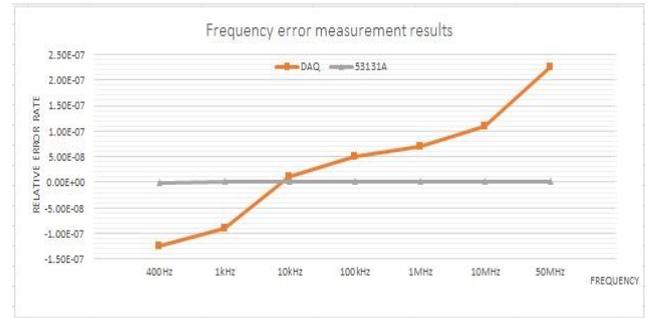


Figure 7. the relative error of frequency measurement result

4.2 Amplitude measurement

Figure 8 is a simulation result about this amplitude measurement method. The measured signal is 3V@DC and 3.1V@2kHz, these result obtained after filtering windowing and FFT calculation shown below (figured by matlab), 2kHz signal amplitude result is 3.1008, the precision to meet the design requirements.

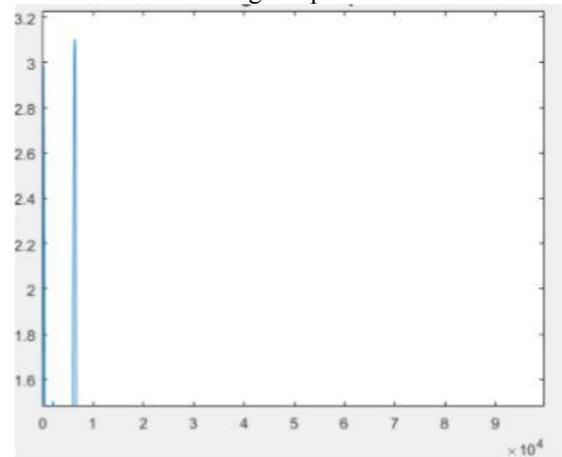


Figure 8. Signal spectrumn by matlab

Figure 9 shows the 400 Hz,1kHz,10kHz actual signal relative error of amplitude measurement results.

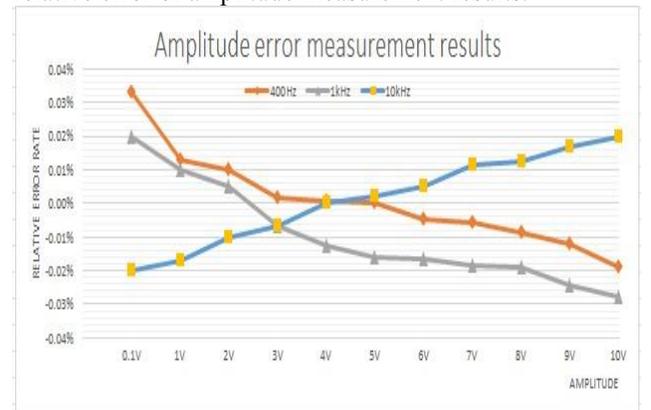


Figure 9. the relative error of amplitude measurement result

5. Summary

All the experiments show that the acquisition system can get more accurate measurement of frequency and amplitude. SoC-based embedded data acquisition system has high integration, high accuracy, and strong performance through experimental verification. The acquisition system for developers to design systems, debugging circuit to bring greater convenience.

6. References

1. Changhong Zhu. "Data acquisition and processing technology". Beijing: Electronic industry Press, 2008,3-20.
2. Jiafu Ren, Xianguo Xi, Yongli Tao, "data acquisition and bus technology". Beijing: Beijing University of Aeronautics and Astronautics Press, 2008,2-50
3. Wei Zheng, "Based on FPGA data acquisition and control system", [Master's thesis] Hubei: Wuhan University of Technology, 2010,1-3
4. Yi Tian, "based system design and implementation of high-speed precision data ARM7 Bian", [Master's thesis] Hebei: Hebei University, 2011,5
5. G. Heinzel A. Rüdiger, Spectrum and spectral density estimation by the Discrete Fourier Transform (DFT), including a comprehensive is of window Functions and some new at-top windows. 2002,2