A Large Bandwidth Differential Cascode Amplifier Cell in InP DHBT for 100-Gb/s Analog Equalizer Applications

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Abstract

This paper reports the design, simulations and measurements of a differential cascode amplifier cell in InP DHBT. From transistor with f_T/f_max reaching 370/340 GHz, this circuit is able to provide a bandwidth of more than 110 GHz, with a maximal differential gain of 9 dB at 90 GHz, and a total peaking of 11 dB. This circuit constitutes a promising building block for analog equalizer structures dedicated to 100-Gb/s optical communication systems.

1. Introduction

With the increasing growth of data communications through past years, we are progressively reaching the limits of data rates. Most current approaches aim at using complex modulation formats such as 64-QAM to increase the spectral efficiency within an optical channel [1]. To achieve data rates beyond 100-Gb/s in on-off keying modulation, which is the simplest way to transmit data, we are faced with the bandwidth limitation of electrical and optical interface at each side of the optical channel, i.e. at the transceiver and the receiver. One of the possible solutions is to use an equalizer to improve the bandwidth of the whole channel thanks to a peaking at high frequencies. Many equalizers have been developed, mainly using CMOS technology to achieve low power consumption and to make them easily tunable [2-4]. However, the main drawback of standard CMOS technologies is limited f_T/f_max, and as a result bandwidth limitation. Moreover, state-of-the-art circuits based on BiCMOS technologies have not yet addressed the 100-GHz-class bandwidth [5-6] which is considered here.

In this paper, we demonstrate a differential cascode amplifier cell targeting 100-GHz-class operation. This circuit is fabricated in a 0.7-um indium phosphide heterojunction bipolar transistor reaching f_T/f_max of 370/340 GHz, achieving a maximal bandwidth of more than 110 GHz, and a maximal peaking of 11 dB at 90 GHz.

In section 2 we present the InP DHBT technology used. The first part of the section 3 describes the design of the differential cascode amplifier and a second part is dedicated to the preliminary simulation results before fabrication. On wafer measurements results are presented in section 4. Conclusions are drawn in section 5.
2. InP DHBT Technology

The differential cascode amplifier cell was designed using III-V Lab’s 0.7-μm InP DHBT technology [7]. This technology provides 5-, 7- and 10-μm emitter-length transistors, with the 5-μm emitter-length mainly used. Figure 1 shows the $f_T/f_{max}$ of the transistor for the various emitter-lengths; best performances are achieved for 5-μm emitter-length, suitable to achieve very large bandwidth circuit. This transistor cannot handle strong currents, but high power output is not needed for this circuit.

![Fig. 1. $f_T/f_{max}$ versus collector current of 5-, 7- and 10-μm emitter-length transistors](image)

3. Differential Cascode Amplifier Cell Design

The differential implementation has been adopted to provide superior insensitivity to power supply parasitic and to double the available swing at the output. As shown in figure 2, the circuit is composed of a differential cascode amplifier with a matching network composed of two stages of emitter followers, in order to provide the optimum DC-level value at the input of the differential cascode amplifier cell (DCAC).

![Fig. 2. Schematic of the differential cascode amplifier](image)

The DCAC uses emitter degeneration by a RC filter at the emitter to ensure a good peaking at high frequency. The choice of the capacitor and the resistor values has been made to maximize the bandwidth while keeping a good value of peaking and a sufficient gain in low frequencies. The simulated influence of the resistor and the capacitor values is shown in figure 3.

![Fig. 3. Influence of the resistor and the capacitor values on the differential response](image)
The biasing of the DCAC is made through a resistor with a negative supply voltage. Although it leads to a non-optimum common mode rejection, this choice has been done to avoid possible instability arising from the use of a transistor-based current source as usually preferred for optimum common mode rejection ratio.

Finally, we designed the layout of the DCAC using Cadence® Virtuoso. 3 levels of metallization are available for routing. The layout has been implemented following many rules. One of the main rules is to minimize interconnects between critical stages, such as between emitter-followers, and between second emitter follower and the DCAC. Another rule is to minimize interconnects between collectors and ground for the emitter followers. To simplify the design, a ground plane using the third level of metallization recovers the entire circuit. This ground plane has two positive aspects: it minimizes the length of grounding interconnects in critical parts, and reduces the inductor effect of all interconnects anywhere in the circuit. Nevertheless, the ground plane does not recover interconnects between the cascode collector and the collector load resistor to benefit from an inductor effect to improve inductive peaking. A compromise has been made for the length of this interconnection to have sufficient inductive peaking while keeping a good output broadband matching. To this end, retro simulations have been performed in order to improve the performance of the circuit.

4. Measurement Results

The S-parameter measurements were performed on wafer with an Anritsu VectorStar® network analyzer, from DC to 110 GHz. We directly process the results to find the differential and common-mode $S_{21}$. Those differential parameters have been calculated thanks to the following equations [8-9]:

\[ S_{dd21} = \frac{1}{2} \cdot (S_{21} - S_{23} - S_{41} + S_{43}) \]  
\[ S_{cc21} = \frac{1}{2} \cdot (S_{21} + S_{23} + S_{41} + S_{43}) \]

Figure 4 shows the resulting values of differential and common-mode $S_{21}$.

![Fig. 4. Mixed-Mode differential (left) and common-mode (right) $S_{21}$](image)

There are four combinations of input and output return loss because of the differential input and output. The input and output return loss are under 0 dB until 110 GHz and under 5 dB until 90 GHz (figure 5). We notice a linear degradation of the output return loss in decibels above 60 GHz, due to the inductive peaking at the collector of the cascode as we explained in the previous section.
5. Conclusion

We reported a very large bandwidth differential cascode amplifier cell with an 11-dB of peaking at 90 GHz. It demonstrates the potential of this architecture in InP DHBT technology to design an equalizer with a very large bandwidth. Future steps include modifying this building block to implement a tunable peaking, e.g. with a varactor [10], in order to equalize various types of optical channel. Another step is the implementation of this building block in a linear feed-forward equalizer in order to obtain a still larger bandwidth.

6. References