A practical integrated 1.5-bit MDAC for pipeline ADCs

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Abstract

A practical integrated 1.5-bit MDAC is introduced which can be used in a pipeline ADC to improve its performances. The MDAC is implemented in a full differential switch-capacitor circuit, which includes a gain-boost amplifier, boot-strapped switches, and pre-amplifying latching comparators. Because of the elaborate design, the MDAC can tolerate the offset of the comparators as high as 1/2LSB with respect to the current stage. The simulated results show that the MDAC achieves a sampling rate of 200MHz with SNR of 76dB and SFDR of 81dB, while consuming only 10.1mW.

1. Introduction

ADCs are widely used in fields such as communication, measurement, medicine and so on [1-4]. In all kinds of ADCs, only pipeline ADCs combine high sampling rate with high resolution [5-9]. MDAC as the crucial block cell of pipeline ADC determines the performances of the whole ADC. In all kinds of MDAC, the 1.5-bit MDAC is the fastest. Because the gain required by the remaining difference amplifier is only 2, the amplifier can achieve broader bandwidth. There are many papers about 1.5-bit MDAC, but no one has given the detailed circuit implementation which an engineer can use in their own design without effort. In this paper a practical implementation of a novel 1.5-bit MDAC is given.

3. Construction

We design the construction shown in figure 1. It is a switch-capacitor circuit whose working cycle has two phases: sampling phase and holding phase. At sampling phase, switches 1 are all closed and switches 2 are open, while at holding phase, it is the contrary case. In figure 1, the three switches, each connected to references signals -1/2Vref, 0, and +1/2Vref, respectively, are controlled by digital code N.

In sampling phase, the three switches are all open; in holding phase, depending one the value of the digital code N, only one of the three switches is closed. If N=0, the switch connected to -1/2Vref is closed, and we have

$$V_{out} = 2\left(V_{in} + \frac{1}{2} V_{ref} \right). \tag{1}$$

If N=1, the switch connected to 0 is closed, we have

$$V_{out} = 2V_{in}. \tag{2}$$

If N=2, the switch connected to 1/2Vref is closed, we have

$$V_{out} = 2\left(V_{in} - \frac{1}{2} V_{ref} \right). \tag{3}$$

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Digital code N is generated by two comparators, whose threshold voltages are set at -1/4Vref and +1/4Vref, respectively. Generally, N is binary encoded. The outputs of the comparators are encoded as

$$N=0, \quad \text{when} \quad -V_{ref} \leqslant V_{in} < -1/4V_{ref}, \tag{4}$$

$$N=1, \quad \text{when} \quad -1/4V_{ref} \leqslant V_{in} < +1/4V_{ref}, \tag{5}$$

$$N=2, \quad \text{when} \quad +1/4V_{ref} \leqslant V_{in} < V_{ref}, \tag{6}$$

Combining (1)-(6), the transfer function shown below is realized:

$$V_{out} = 2\left(V_{in} + \frac{1}{2}V_{ref}\right), \qquad -V_{ref} \leqslant V_{in} < -1/4V_{ref}; \tag{7}$$

$$V_{out} = 2V_{in}, \qquad -1/4V_{ref} \leqslant V_{in} < +1/4V_{ref}; \tag{8}$$

$$V_{out} = 2\left(V_{in} - \frac{1}{2}V_{ref}\right), \qquad +1/4V_{ref} \leqslant V_{in} < V_{ref}. \tag{9}$$

which is the transfer function of a 1.5-bit MDAC. From (7)-(8), we find that the MDAC can tolerate the offset of the comparators as high as 1/2LSB with respect to the current stage.

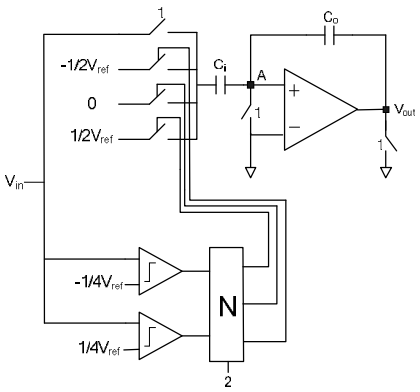

Figure 1. Single-ended 1.5-bit MDAC

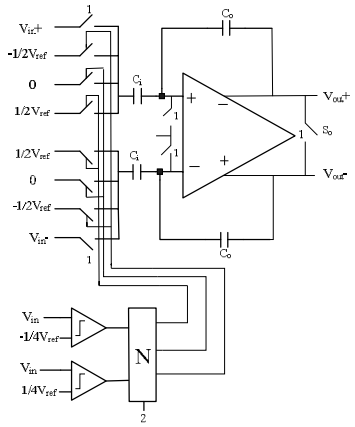

Figure 2. Full differential 1.5-bit MDAC

As we know, the single-ended signaling is disadvantage of being susceptible to common noises such as power supply noise, common glitches, common switch noises, and so on. In order to get better performance, we transfer the single-ended construction shown in figure 1 into the full differential one as shown in figure 2.

4. Circuit

As shown in figure 3, the amplifier used to multiply the remaining difference is a folded cascode construction. In order to minimize the input noise, the PMOS differential pair is used for input transistors.

In order to improve linearity, the gain-boost technique is used to multiply the gain of the amplifier, so the gain of the whole circuit can be expressed as:

$$G = \frac{g_{mp1} g_{mn4} r_{on1} r_{on4} G_2 g_{mp7} r_{op7} r_{op5} G_2}{g_{mn4} r_{on1} r_{on4} G_2 + g_{mp7} r_{op7} r_{op5} G_2}, \tag{10}$$

where gmp1, gmp7, and gmn4 are the transconductance of P1, P7 and N4, respectively; ron1, ron4, rop7, and rop5 are the output resistance of transistors N3, N4, P7 and P8, respectively; G1 and G2 are the gain of amplifiers A1 and A2, respectively. The common output signal is decided by the common feedback circuit.

Shown in figure 4 is the proposed pre-amplifying and latching comparator, which consists of a preamplifier followed by a latch. The preamplifier amplifies the minus difference between the signal and the reference, and the latch latches the compared result of the signal with the reference.

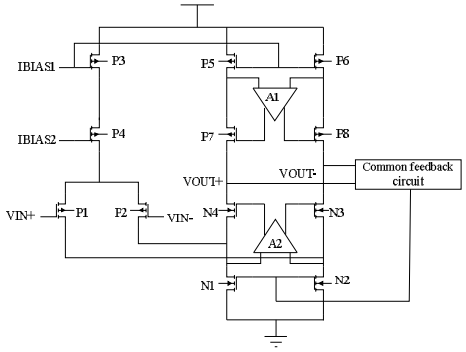

Figure 3. Remaining difference amplifier

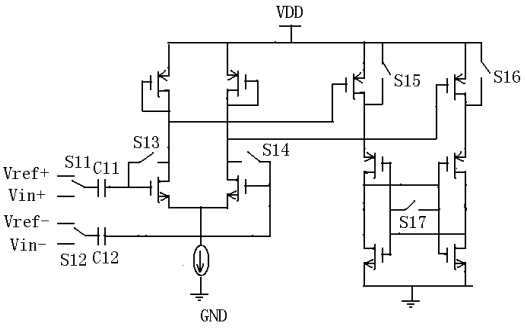

Figure 4. Pre-amplifying and latching comparator

The work process of the comparator consists of two steps corresponding the two phases of the MDAC. At the holding phase, the two-throw switches S11 and S12 are thrown to the reference signals Vref+ and Vref- and the two resetting switches S13 and S14 are closed, so the reference signals are sampled onto the capacitor C11 and C12 and the preamplifier is reset. Switches S15 and S16 are closed and S17 is open; the latch is in its latching state. At the sampling phase, two-throw switches S11 and S12 are thrown to the analog signals and switches S13 and S14 are open. The analog signal Vin+ - Vin- is compared with the reference Vref+-Vref- which has been sampled at the capacitors at the holding step. The difference is amplified by the preamplifier. Meanwhile, switches S15 and S16 are open and switch S17 are close. The latch acts as a load for the preamplifier. At the end of sampling phase, the switches S15 and S16 begin to close and the switch S17 begins to open initiating the latch to latch the instant state. The output of the latch is then encoded into digital signal N as shown in figure 2.

5. The simulation

We have simulated the 1.5-bit MDAC using a professional CAD program. The simulated wave is shown in figure 5.

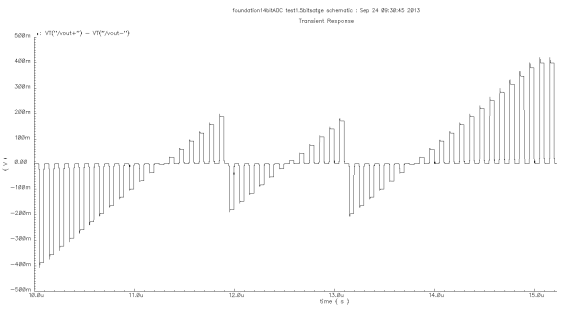

Figure 5. Simulated wave of 1.5-bit MDAC

The half-period zero-returning is caused by switch S_o closing during sampling phase in figure 2, which can partially eliminate the charge memory effect of the feedback capacitors. From the simulated wave in figure 5, we find

that the transfer function of 1.5-bit MDAC is realized. Further simulation shows that the MDAC achieves a sampling rate of 200MHz, with SNR of 76dB and SFDR of 81dB, while consuming only 10.1mW power.

6. Conclusion

A practical 1.5-bit MDAC is introduced in this paper. The 1.5-bit MDAC can tolerate the offset of the comparator as high as 1/2LSB. A special switch-capacitor circuit is designed to implement 1.5-bit MDAC, which includes a gain-boost amplifier, boot-strapped switches, and pre-amplifying latching comparators. The simulated results show that the MDAC achieves a sampling rate of 200MHz, with SNR of 76dB and SFDR of 81dB, while consuming only 10.1mW power.

8. References

1. J. Li and U. Moon "A 1.8 V 67 mW 10-bit 100 Ms/s pipelined ADC using time shifted CDS technique", IEEE J. Solid-State Circuits, vol. 39, no. 9, pp.1468 -1476 2004.

2. B. Lee , B. Min , G. Manganarom and J. W. Valvano "A 14-b 100-MS/s pipelined ADC with a merged SHA and first MDAC", IEEE J. Solid- State Circuits, vol. 43, no. 12, pp.2613 -2619 2008.

4. J. Arias , V. Boccuzzi , L. Enriquez , D. Bisbal , M. Banu and J. Barbolla "Low-power pipeline ADC for wireless LANs", IEEE J. Solid-State Circuits, vol. 39, no. 8, pp.1338 -1340 2004.

5. B. Min , P. Kim , F. W. Bowman III, D. M. Boisvert and A. J. Aude "A 69 mW 10-bit 80-MSample/s pipelined CMOS ADC", IEEE J. Solid-State Circuits, vol. 38, no. 12, pp.2031 -2039 2003.

6. D. Kurose , T. Ito , T. Ueno , T. Yamaji and T. Itakura "55-mW 200-MSPS 10-bit pipeline ADCs for wireless receivers", IEEE J. Solid-State Circuits, vol. 41, no. 7, pp.1589 -1595 2006.

7. P. Wu , V. Luen and H. Luong "A 1 V 100-MS/s 8 bit CMOS switched- opamp pipelined ADC using loading free architecture", IEEE J. Solid-State Circuits, vol. 42, no. 4, pp.730 -738 2007.

8. Ahmed, I., Johns, D.A., "A High Bandwidth Power Scalable Sub-Sampling 10-Bit Pipelined ADC With Embedded Sample and Hold", Solid-State Circuits, IEEE Journal of, On page(s): 1638 - 1647, Volume: 43 Issue: 7, July 2008.

9. Chun C. Lee, and Michael P. Flynn, "A SAR-Assisted Two-Stage Pipeline ADC", IEEE JOURNAL OF SOLID-STATE CIRCUITS, On page(s): 859 - 869, VOL. 46, NO. 4, APRIL 2011.

10. A. Varzaghani and C.-K. K. Yang, “A 600 MS/s, 5-bit pipelined analog-to-digital converter for serial-link applications,” in Symp. VLSI Circuits Dig., 2004, pp. 276–279.