Cylindrical Substrate Integrated Waveguide (CSIW) Slot Arrays with Uniform and Nonuniform Spacings

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Abstract

Pattern synthesis of a traveling wave longitudinal slot array on the broad wall of cylindrical substrate integrated waveguide (CSIW) is presented at 25 GHz. In order to have low side lobe level (SLL) and high directivity, the Elliot's design procedure for 1 x 25 slotted waveguide array is applied to satisfy the required slot voltage distribution found by aperture projection method for evenly distributed slot array with complex slot voltage distribution. The results are compared with the design which makes use of only the phase compensation of the resonant slots using non-uniform spacing to obtain high directivity. The advantages and disadvantages of both designs are compared in terms of the design procedure and electrical performance. CSIW array with nonuniform spacing has been fabricated and measured. Reasonable agreement between the simulation and measurement results is observed.

1. Introduction

Slotted waveguide arrays provide low loss, high isolation and high power handling and they are widely used in communication and radar applications due to those advantages. Some of the applications require conformal antennas in which the shape of the antenna is determined by the considerations other than electromagnetics [1]. The substrate integrated waveguide (SIW) recently proposed in the literature [2] seems to be suitable for conformal slotted waveguide applications because SIW has both the advantages of waveguides and the microstrip technology. Although SIW has dielectric losses, it can be easily conformed to any surface when a flexible substrate is used and this makes SIW technology attractive for conformal array applications. Most of the conformal slotted waveguide arrays in the literature are composed of regular rectangular waveguides. A traveling wave slotted SIW array conformed circumferentially on a cylinder has been introduced in [3 - 5]. In this paper, two different traveling wave conformal longitudinal slot array configurations are examined and compared. One of the standard pattern synthesis methods, the aperture projection method is applied to obtain both low side lobe level (SLL) and half power beam width (HPBW). In the first configuration, nonuniform slot separations are used with resonant slots, while in the second configuration array elements are spaced uniformly.

2. Non-Uniform Resonant Slot Array

Schematic view of a slot array on SIW conformed circumferentially around a cylinder is shown in Figure 1. The slot width is chosen as 0.25mm in order to satisfy narrow slot assumption in the Elliott's design procedure [6]. The radius of CSIW is 10 cm. The slot characterization is carried out as described in [3]. The array is excited from Port 1 and Port 2 is terminated by a matched load. The first element in the array is the element closest to the matched load. A 1x16 slot array on CSIW (R=10cm) is designed at 25 GHz on 0.5 mm thick Rogers 3003 substrate (ε_r = 3, tanδ = 0.0013 @ 10 GHz) with non-uniform slot separation values. The slot separation values are adjusted to compensate the spatial phase delay of the slot elements for the main beam along the broadside direction. 16 slot elements are chosen to have nearly the same angular coverage with the 25 slot array presented in Section 3. A -20 dB SLL Taylor (ñ=3) amplitude taper is used

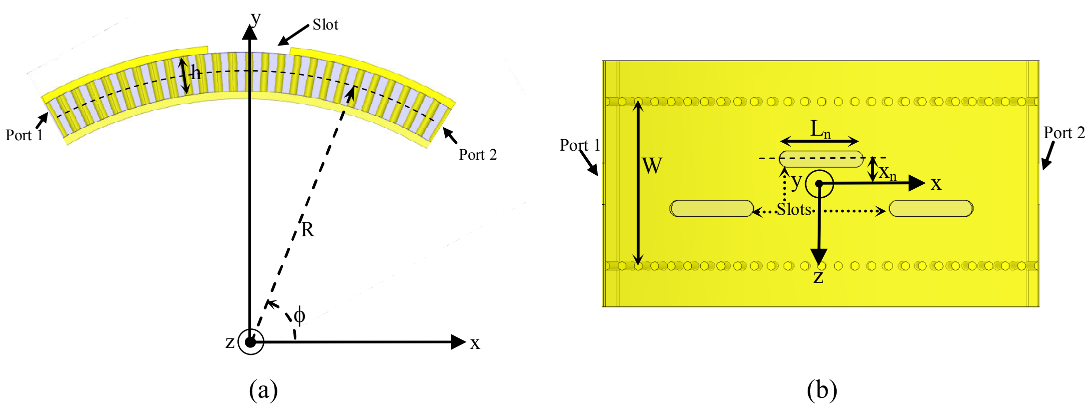

Figure 1. Longitudinal slot array on broad wall of CSIW: (a) Cross-sectional and (b) top views.

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to determine the amplitude taper of the slots. It is observed that some of the separation values are quite larger than $\lambda_0/2$, which causes significant increase in some of the side lobes.

To suppress these side lobes, the slot lengths and offsets are optimized. In the optimization, it is allowed that some successive slots are not alternated as in [5]. However, SLL around -10 dB is achieved in the simulations. The optimized 16 element slot array is fabricated using standard printed circuit board (PCB) technology and the picture of the fabricated array is presented in Figure 2 (a). The measured s-parameters of 1 x 16 slot array are presented in Figure 2 (b) & (c). It is observed that, there is quite good agreement between the simulated and measured results. The antenna is measured in anechoic chamber by placing it on a cylindrical foam with R=10cm as shown in Figure 3 (a). The measured radiation pattern of 1 x 16 slot array at 25 GHz is compared with the simulations in Figure 3 (b). Good agreement between the measured and simulated radiation patterns results is obtained. The HPBWs of the measured and simulated patterns are about 5.19° and 5.59°, respectively. There are small differences between the some of the SLL values which might be caused by the errors in locating the array on flexible foam support.

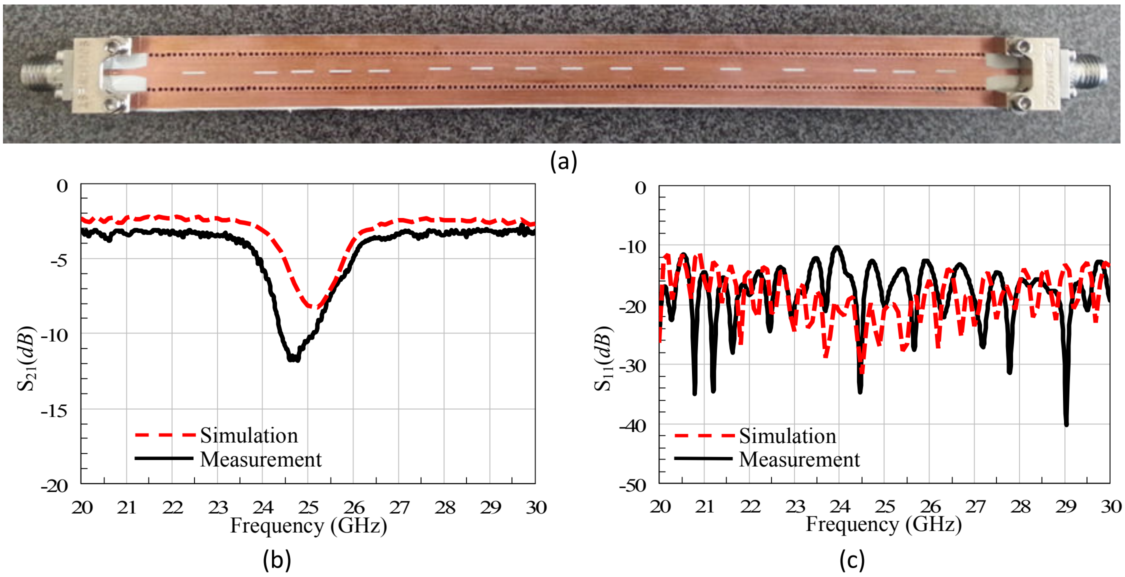
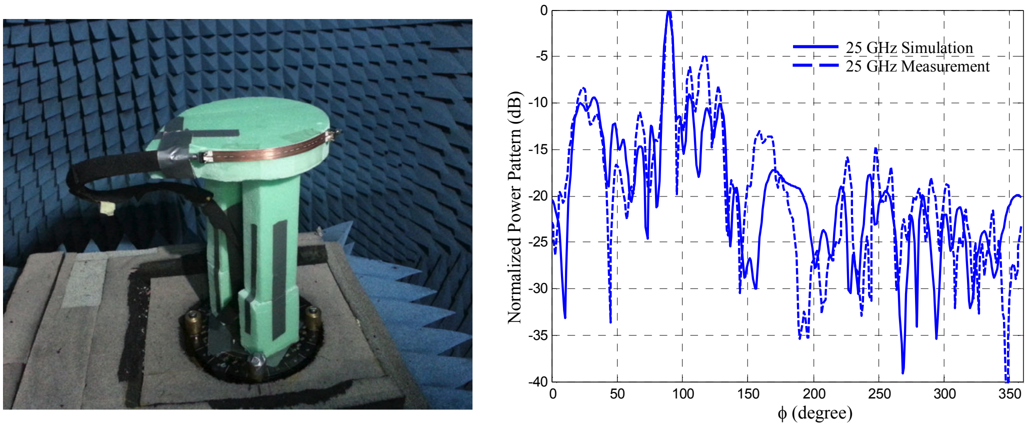


Figure 2. (a) Fabricated 1x16 slot array. (b) & (c) Comparison of the simulated and measured s-parameters.



(a) (b)

Figure 3. (a) Measurement setup of 1 x 16 slot array on CSIW (R = 10 cm). (b) Radiation patterns of 1 x 16 slot array.

3. Uniform Slot Array

To achieve low SLL pattern, uniformly spaced array configuration is preferred in the design of the second array. In this array, most of the slot elements are at out of resonance. There are a limited number of studies which employs the design of the slots out of resonance to satisfy complex slot voltage distribution of the slots [7].

The aperture projection method is used to determine the excitation voltages of the uniformly distributed slots. The 25 element slot array is formed on h = 0.5 mm thick Rogers 3003 substrate. The slot elements are uniformly spaced with $0.7\lambda_g$ spacing on the CSIW with R=10 cm. The SLL design requirement is -20 dB. The amplitudes of the slot voltages (V_s) are determined by sampling -20 dB SLL Taylor ($\tilde{n}$ = 3) line source distribution along the x-axis at the projected positions of the array on the x-axis as shown in Figure 4. The sampled array weights are adjusted further by taking the element density and the element factor into account [8]. The phases, ψ_n, of the cylindrical slot array elements are

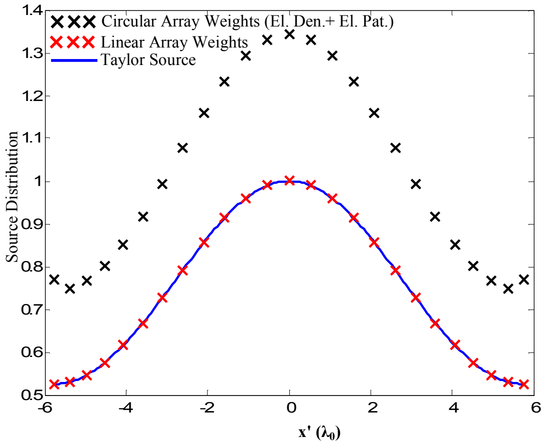
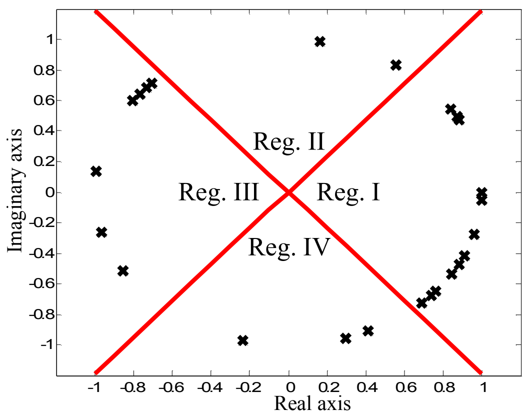


Figure 4. Sampling Taylor line source distribution using projected aperture positions.

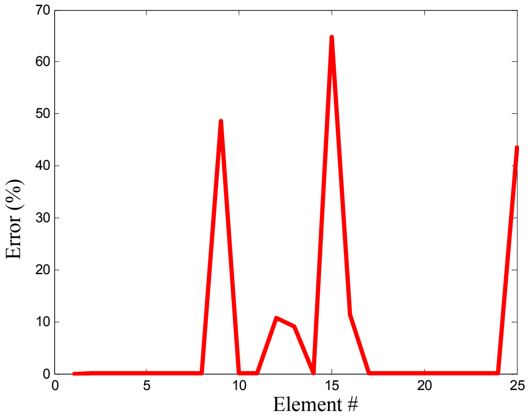
determined to compensate the different path lengths to obtain in phase contribution from each element to rotate the beam. Differences between the slot voltage phases ψ_n, calculated by aperture projection method and phases of the traveling wave mode in CSIW, φ_n, are determined. exp(j(ψ_n -φ_n) are plotted in Figure 5 (a). The required slot voltages cannot be achieved by using only resonant slot elements. Thus, one of the elements in the array is chosen as a resonant slot. The angular values in Figure 5 (a) can be considered as the deviations of the slots from the resonance. In Figure 5 (a), four regions are constructed by considering the ±50° deviation from the resonance which is considered to be safe enough in order to avoid numerical problems and in order not to decrease radiation efficiency of the array consisting out of resonance slots [7]. Hence, the deviations of the slot voltages from the mode voltages are desired to be within Region I and III. The first slot on the array is chosen as a resonant slot. Changing the resonant element in the array causes the rotation of the phase points in Figure 5 (a). The required slot phases are chosen by minimizing the number of points in Region II and IV. When most of the elements are kept in Region I and III, it is observed that main beam deviates from broadside by a few degrees, which is 2° in the presented design.

The Elliot's design procedure is applied [6] to determine the slot offsets and lengths which correspond to the slot voltage excitation. The external and internal couplings are approximated by considering the planar slotted SIW in the design. The error in the calculated slot admittance values in the Elliot's design procedure is given in Figure 5 (b). As it is seen in Figure 5 (b), there are in total 5 high error points for the elements which correspond to the 5 improper points in Figure 5 (a) lying outside the Region I and III.

Using the calculated slot offsets and lengths, 1x25 longitudinal slot array on CSIW is simulated at in Ansys HFSS (high frequency structure simulator). The simulated slot voltage amplitudes and phases at 25 GHz are compared with the desired -20 dB SLL Taylor (ñ=3) distribution in Figure 6 (a) and (b), respectively. In Figure 6 (a), there are some deviations in the simulated slot voltage amplitude terms while the slot voltage phases shown in Figure 6 (b) is in a quite good agreement with the desired one. Moreover, in the design procedure the mutual couplings are approximated by the planar SIW case and the effect of the dielectric losses are not taken into account. Whereas in the simulations, both curvature effects and dielectric losses are included. The simulated return loss is -13.2 dB and power delivered to load is %4.8 in the simulations while they are calculated in the Elliot's design procedure as -11.3 dB and %8.47, respectively. Due to the dielectric losses power delivered to load reduces in the simulations. Simulated radiation pattern of the array is given in Figure 7. It is observed SLL is almost below -20 dB. There is one side lobe near the main beam around -18 dB. The simulated HPBW in Figure 7 is about 4.8°. This array is in fabrication. Measurement results will be presented in the conference.

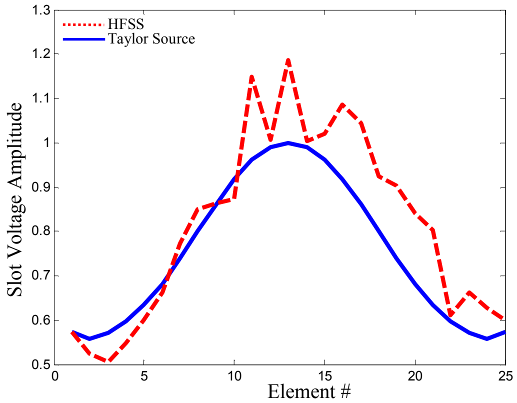


(a)

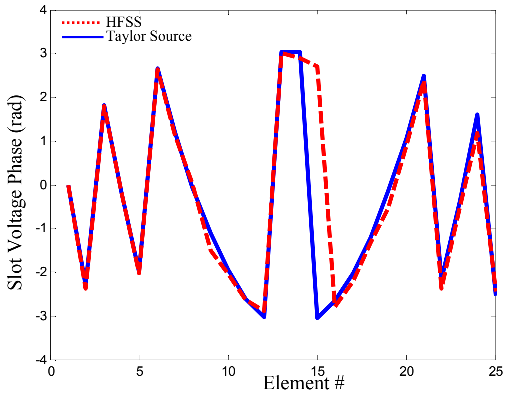


(b)

Figure 5. (a) Plot of exp(j(ψ_n -φ_n) on complex plane; ψ_n :the slot voltage phases calculated by aperture projection method and $\varphi_{n:}$ phases of the traveling wave mode in CSIW (b) Error in the calculated slot admittances by Elliot's design with respect to required values.



(a)



(b)

Figure 6. Comparison of the calculated and desired slot voltage (black curve in Figure 4) (a) amplitudes and (b) phases (25 GHz).

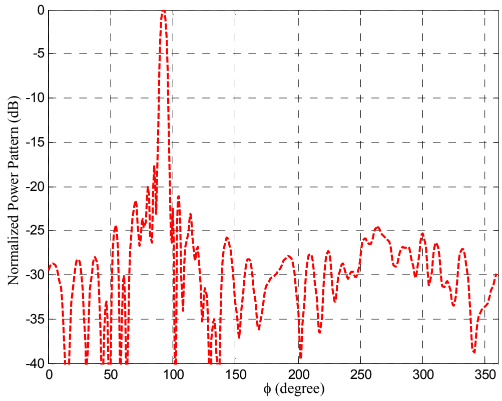


Figure 7. H-plane radiation pattern of 1x25 traveling wave slot array simulated at 25 GHz on CSIW (R=10cm).

4. Conclusion

The aperture projection method is applied to the uniformly distributed 1 x 25 slot array on CSIW to have low SLL pattern. Complex slot voltage distribution is used to achieve low HPBW values together with low SLL. The difficulties with using non-resonant slot elements in the design are discussed. The design is compared with 1 x 16 slot array using resonant slot elements. It is seen that the nearly the same HPBW can be obtained with the resonant slot array but desired SLL cannot be reached due to non-uniform slot separation values. Although design with nonuniform spacings makes use of resonant slot arrays (presented in Section 2) which is not vulnerable to the design difficulties caused by the complex slot voltage distribution as described in Section 3, this method does not give the controlled SLL design.

5. Acknowledgments

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6. References

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