A precision spectrometer for measuring signals from the Epoch of Cosmological Recombination

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Abstract

The rapid advances in processing capabilities of modern Field Programmable Gate Array (FPGAs) combined with high-speed analog-to-digital converters (ADC) make high-resolution, high dynamic range spectroscopy for verifying the signature of the Epoch of Recombination possible. A prototype 4 GHz precision spectrometer, based on quadrature sampling of analog signals followed by an efficient, parallelizable FFT architecture amenable to implementation inside an FPGA is described. Quadrature sampling of two analog signals, each having a bandwidth of about 2 GHz, is implemented using 10-bit, time-interleaved ADCs that has features for correction of gain, offset and phase mismatches. A combination of pipelined FFT IP-cores and a custom-designed parallel FFT engine provide 8192 spectral channels across each of the 2 GHz bands. Since the spectral purity of the sampling clock is an important consideration in precision applications, the effect of normally distributed jitter in the sampling clock on the deviations from a flat spectrum while sampling a band-limited white noise is presented.

1. Introduction

The Cosmic Microwave Background (CMB), the relic thermal radiation that fills the Universe, is thought to be the earliest light in the Universe, tracing its origins back to the Big Bang. After the Big Bang, the matter in the Universe consisted of highly ionized plasma. The Epoch of Recombination refers to that period in cosmological evolution when the hot plasma content of the early Universe gradually transitioned to the atomic state as the Universe expanded and cooled. The photons released during this process are predicted to manifest as 'ripples' in wideband spectra of the cosmic radio background, since recombination of the primeval plasma in the early Universe adds broad spectral lines to the relic Cosmic Radiation. The lines are extremely wide because recombination is stalled and extended over redshift space. The spectral features are expected to be isotropic over the whole sky.

Experimentally, verifying the signature of the Epoch of Recombination in the CMB spectrum is extremely challenging since the estimated magnitude of fluctuations is 8 to 9 orders of magnitude weaker than the CMB radiation temperature. However, modern technology has brought the investigation of these predictions to the threshold of experimental astronomy by allowing development of high-sensitivity, wide band radio telescopes. The Raman Research Institute has embarked upon building the **A**rray of **P**recision **S**pectrometers for the **E**poch of **R**ecombin**A**tion-APSERa – a project to detect recombination lines from the Epoch of Cosmological Recombination. This project shall comprise of an array of 128 small telescopes that are purpose-built to detect a set of adjacent lines from cosmological recombination in the spectrum of the radio sky in the 2-6 GHz range. As part of APSERa, wide band, Fast Fourier Transform (FFT) based precision Spectrometer (pSPEC) to sample and process analog signals of bandwidth of about 4 GHz are being developed.

2. Precision spectrometer for APSERa

The pSPEC unit shall form the digital back-end receiver of APSERa. A prototype pSPEC was developed to demonstrate a digital receiver capable of quadrature sampling of two analog signals- each having a bandwidth of about 2 GHz- using high-speed time-interleaved (TI) commercial ADCs, and implement 8192-point FFT engines using modern FPGAs. It is built around two, quad 10-bit ADCs, (EV10AQ190CTPY) from e2V technologies and a Virtex6 (XC6VLX240T) FPGA, laid out on an 18-layer mixed-signal board. To stream data out of pSPEC, it has provision for multiple gigabit Ethernet and 4.5 Gbps fibre optic interfaces. Figure-1 shows a block diagram and a photograph of prototype pSPEC-unit.

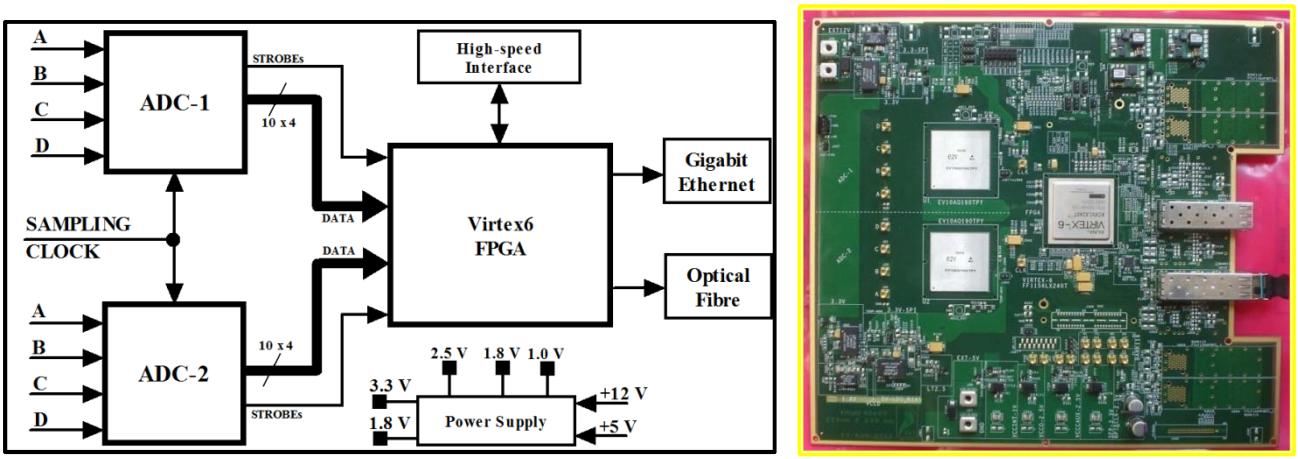

Figure-1: A block diagram and a photograph of pSPEC-unit

The individual cores of the quad ADC, having an analog input bandwidth of about 3 GHz, is capable of sampling analog signals up to 1.25 GSps. Since the requirement is to sample two, quadrature (I-Q) analog signals, each having a bandwidth of about 2 GHz, ADCs are configured to time-interleave in groups of two, thereby, effectively sampling at 2 GSps. While time-interleaving facilitates sampling of broadband signals, distortion products (spurs) as a result of gain-, phase-, bandwidth- and offset-mismatch between time-interleaved ADC channels present a significant challenge in optimal utilization of ADC's capability. These challenges could be met by leveraging the combination of ADC's on-chip compensation features, matching of flight-times of signals routed between ADCs and FPGA to within timing-budget limits, and path delay-adjustment features inside the FPGA. In order to evaluate the performance of TI-ADCs on pSPEC and test the purpose-developed data-grabbing firmware at 500 MSps double data rate, a tone at a frequency of 156.25 MHz was fed to one of the time-interleaved ADC groups.

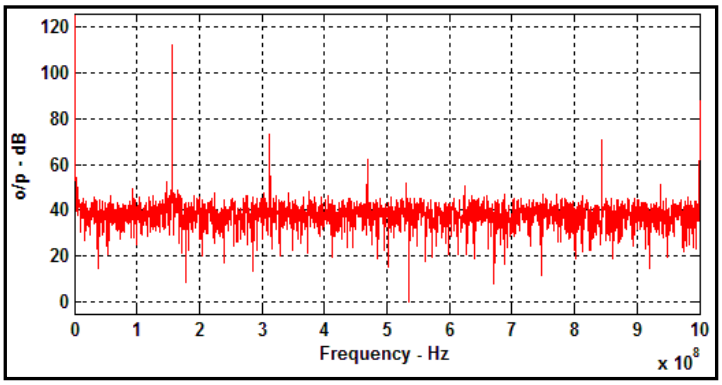

Figure-2: Spectrum of two, time-interleaved ADCs

Figure-2 shows the spectrum obtained by offline transformation of data samples obtained from two time-interleaved ADCs operating at 2 GSps. The spurious-free dynamic-range, which is measured to be better than 55 dBc, compares favourably with the datasheet specification of ADC in TI mode of operation.

An important consideration in the design of high-speed ADC boards is the spectral purity of the sampling clock. A traditional way of quantifying jitter in the sampling clock is by specifying its phase noise. To arrive at a phase noise value which is permissible for pSPEC, we have studied the effect of normally distributed jitter in the sampling clock on the deviations in the pass band characteristics of band limited white noise While it is straight-forward to introduce the effect of random jitter in the sampling clock on the digitized tone, it is not so for digitizing a band of noise. In this case, it may be advantageous to work in the autocorrelation domain, wherein, each sample of the autocorrelation function (ACF) is perturbed using normally distributed jitter. To estimate the effect of sampling jitter on the band pass, we have averaged 2048 perturbed ACFs. While the averaging process reduces the peak value of ACF from one, the nulls in the autocorrelation function do not average to zero due to the asymmetric nature of the ACF around each null. The resulting bias due to averaging alternates between positive and negative values for odd and even nulls.

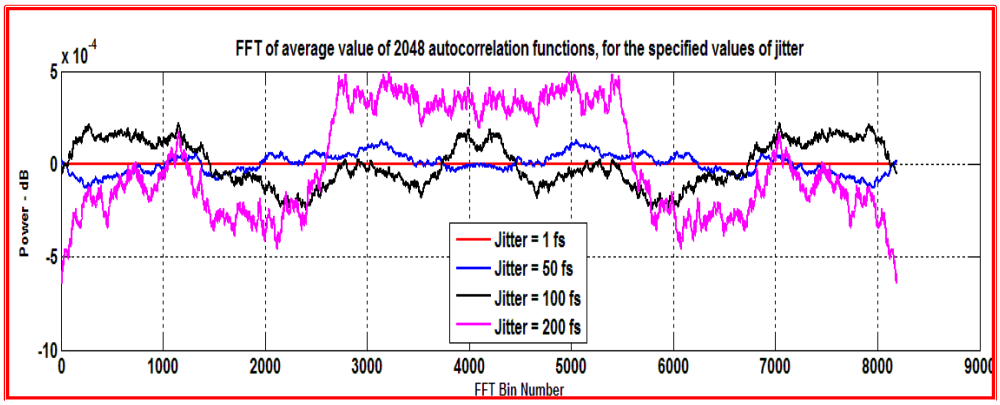

Figure-3: Variations in flatness of pass band as a function of jitter in sampling clock

Figure-3 shows variations in the flatness of the pass band due to the combination of jitter ranging from 1 fs to 200 fs in sampling the autocorrelation function and bias of the autocorrelation function around the nulls.

While the peak-to-peak variation in the pass band for a jitter of 200 fs is within 0.001 dB, the same for a jitter of 1 fs is within 6e-6 dB. According to ADC datasheet, the total jitter in the sampling clock should be around 100 fs. The sampling clock source used with the prototype pSPEC unit has a typial (rms) jitter of about 70 fs. While it meets the short-term stability of pSPEC clock source, the long-term stability could be achieved by disciplining it using a reference signal derived from a GPS receiver. However, when the same sampling clock source is used to sample broadband noise input, a peak-to-peak ripple of about 4e-4 dB could be seen in the passband.

3. Signal processing inside the FPGA of pSPEC

Advances in process technology have allowed modern FPGAs to increase their density, performance, and provide faster interfaces. This has enabled parallelization of algorithms required to implement large bandwidth, high-resolution spectrometer for radio astronomical applications. Figure-4 shows one of the two identical signal-flow paths of pSPEC's firmware, consisting of 8192-point FFT engine and detection and accumulation logic to compute power spectra for user-defined integration period. The 8192-point FFT is realised as (M**x**N)-point FFT, in which a combination of eight, parallel, pipelined FFT IP-cores from Xilinx and a custom-designed 8-point parallel FFT engine have been used. In order to reduce the finite word-length effects, bit-precision at different stages of the design is chosen optimally based on power-level maintained at the input port of ADCs. The power-levels could be set in such a way that there are sufficient bits to represent the sky signal with negligible non-linearity and simultaneously allowing sufficient headroom to realise a high dynamic-range, RFI-tolerant spectrometer.

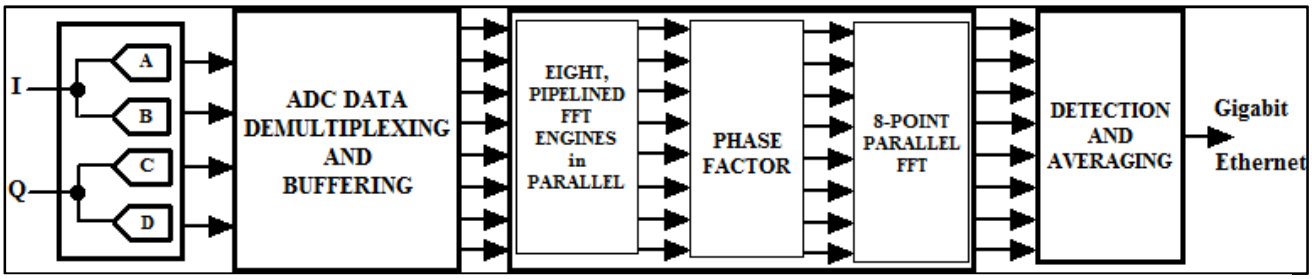

Figure-4: Signal-flow diagram of pSPEC

In addition, considering that a large bandwidth is processed inside the FPGA, accumulation of power spectra reduces the output data transfer rates, thereby, reducing load on external interface and data storage requirements. Using the gigabit Ethernet interface, spectra, integrated on-chip for a period of ~ 16 milliseconds, are streamed out of pSPEC at 25 MBps. In order to test the functionality of the 8192-point FFT architecture developed for pSPEC, broadband noise, filtered using a low-pass filter (F_c = 450 MHz), was fed to one of the groups of time-interleaved ADCs and sampled at 2 GSps. The 8192-point FFT spectrum obtained for the above input conditions is as shown in Figure-5.

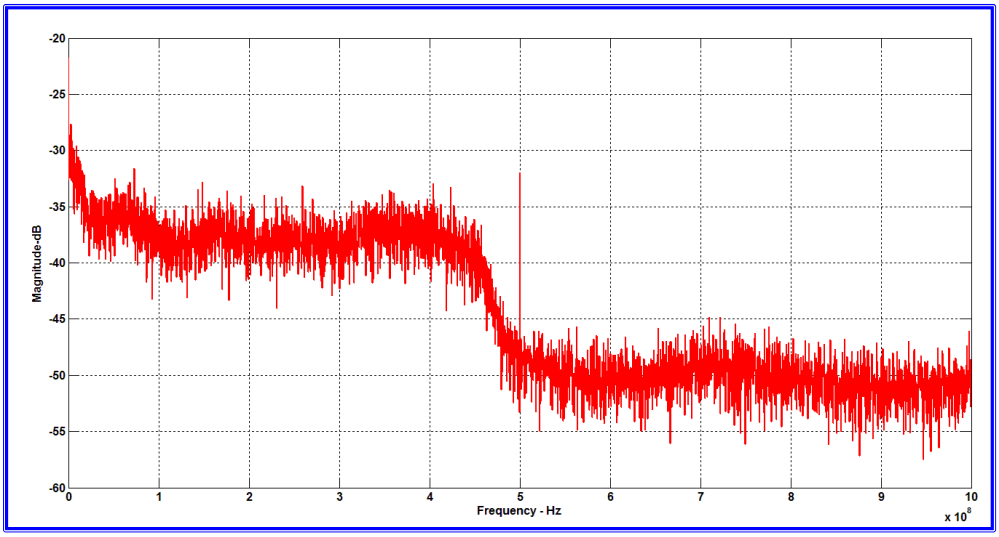

Figure-5: Spectrum obtained from 8192-point FFT for band-limited noise input

4. Conclusion

As part of the APSERa project, a prototype pSPEC unit, capable of quadrature sampling of two analog signals, each of about 2 GHz bandwidth, and digital processing of the same has been designed and developed. As shown in Figure-2 and Figure-5, firmware to grab high-speed data from ADCs operating in time-interleaved mode and evaluation of time-interleaved ADCs along with implementation of parallelized architecture of an 8192-point FFT have been realised. In the study on the effects of sampling clock jitter on the pass band characteristics while sampling a band limited white noise, it was found that a peak-to-peak ripple of about 4e-4 dB could be seen in the passband. The process of integrating the detection and accumulation section of the FPGA firmware and evaluation of the precision spectrometer is being carried out. When the prototype pSPEC unit is integrated with other sub-systems of APSERa to carry-out integrated testing at a suitable location, it is intended to replace the 8192-point FFT with a polyphase filter bank.

5. Acknowledgement

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