

# A 60-GHz On-Chip Antenna Over an AMC Using a Standard 65-nm CMOS Technology

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**Abstract**—This paper presents a design process and simulation results of a U-shaped antenna over an artificial magnetic conductor (AMC) using a standard 65-nm CMOS technology for 60-GHz frequency band applications. The structure of the proposed on-chip antenna consists of a U-shaped monopole antenna fed with conductor-backed CPW line at the terminal aluminum layer LB and a novel AMC constructed with M1 to M6 metal layers. Ansoft HFSS is used for design simulation. Based on the simulated results after optimization, the U-shaped CPW-fed monopole antenna mounted on the AMC can offer higher gain and wider impedance bandwidth while maintaining an electrical size reduction.

**Index Terms** --- 60-GHz, Artificial Magnetic Conductor (AMC), Complementary metal-oxide semiconductor (CMOS), perfect magnetic conductor (PMC), vertical natural capacitor (VNCAP)

## I. INTRODUCTION

During the past decade, the 60-GHz band has emerged as one of the most promising candidates for multi-gigabit wireless applications due to its various advantages over currently proposed or existing communication systems. These advantages include huge unlicensed bandwidths (up to 9 GHz) and less restricted regulation in terms of power limits [1]. With the performance improvement in advanced standard CMOS technology and the short wavelength of the electromagnetic waves at 60-GHz band, there is an opportunity to implement a low-cost and compact fully integrated 60-GHz transceiver system on a single chip [2]-[3].

As a key role in the 60-GHz transceiver system, an on-chip antenna with effective performance and a small size is essential. However, in standard CMOS process, the low-resistivity silicon substrate is in general not optimized for on-chip antennas particularly at high frequencies like 60-GHz band, at the same time, the horizontal dimension is limited to be used and the vertical space is also locked in by the particular fab process. Thus, there are many challenges to achieve the successful integration with standard CMOS technology [4]. Although a few approaches were presented to improve the radiation efficiency of the on-chip antenna, such as micromachining process and proton implantation [5]-[6],

but these techniques are more expensive, complex and not compatible with the mainstream CMOS Process.

AMC structures have gained great attention in low-profile wire antenna designs in recent years due to their ability to present the same properties as a perfect magnetic conductor (PMC) within a certain frequency band, exhibiting  $0^\circ$  reflection phase at the resonance frequency and resulting in good radiation efficiency [4][7]. In this paper, a U-shaped on-chip antenna over a vertical natural capacitor (VNCAP) loading AMC is designed using 65nm standard CMOS process. The loaded VNCAP could reduce the size of AMC unit cell for compact. High Frequency Structure Simulator (HFSS) is used for the simulation. The proposed on-chip antenna placed on the novel AMC is optimized to cover from 57 to 66 GHz.

## II. ON-CHIP ANTENNA DESIGN OVER A NOVEL AMC

In this on-chip antenna design, a commercial standard 65nm CMOS process with thick metallization scheme is used. Fig. 1 shows the cross section view of the metallization option in standard 65 nm CMOS technology. M1 to LM are copper levels and LB is terminal aluminum layer. The metal layers are embedded between insulator layers on/above the bulk silicon substrate. The insulator layers ( $\text{SiO}_2$ ) and the passivation layers are all modeled as lossless (conductivity  $\sigma = 0$  siemens/m).

### A. Square patch with VNCAP loading AMC unit cell design

An AMC is usually an infinite array of AMC unit-cell structures over a ground plane realized by periodic arrangement. The reflection phase of an AMC for plane wave incidence is a function of frequency decreasing continuously from  $180^\circ$  to  $-180^\circ$  as frequency increases and its value is  $0^\circ$  at the resonance frequency. The AMC's bandwidth is generally chosen by the  $+90^\circ/-90^\circ$  reflection phase points according to convention because these points define the 3 dB gain roll-off for a horizontal current source placed just atop the AMC surface.

	$\epsilon_r=3.4$ , thickness= $0.475\mu\text{m}$	
	$\epsilon_r=7.0$ , thickness= $0.4\mu\text{m}$	
LB	$\epsilon_r=4.1$ , thickness= $1.775\mu\text{m}$	
	$\epsilon_r=4.4$ , thickness= $1.45\mu\text{m}$	VV
LM	$\epsilon_r=4.1$ , thickness= $3.3\mu\text{m}$	
	$\epsilon_r=4.4$ , thickness= $0.6\mu\text{m}$	V7
M7	$\epsilon_r=3.6$ , thickness= $0.9\mu\text{m}$	
	$\epsilon_r=4.0$ , thickness= $0.6\mu\text{m}$	V6
M6	$\epsilon_r=3.0$ , thickness= $0.22\mu\text{m}$	
	$\epsilon_r=3.292$ , thickness= $0.167\mu\text{m}$	V5
M5	$\epsilon_r=3.0$ , thickness= $0.22\mu\text{m}$	
	$\epsilon_r=3.292$ , thickness= $0.167\mu\text{m}$	V4
M4	$\epsilon_r=3.0$ , thickness= $0.22\mu\text{m}$	
	$\epsilon_r=3.292$ , thickness= $0.167\mu\text{m}$	V3
M3	$\epsilon_r=3.0$ , thickness= $0.22\mu\text{m}$	
	$\epsilon_r=3.292$ , thickness= $0.167\mu\text{m}$	V2
M2	$\epsilon_r=3.0$ , thickness= $0.22\mu\text{m}$	
	$\epsilon_r=3.292$ , thickness= $0.167\mu\text{m}$	V1
M1	$\epsilon_r=3.237$ , thickness= $0.22\mu\text{m}$	
	$\epsilon_r=4.45$ , thickness= $0.291\mu\text{m}$	
	$\epsilon_r=4.1$ , thickness= $0.289\mu\text{m}$	
Substrate: $\epsilon_r=11.9$ , thickness= $280\mu\text{m}$ , conductivity $\rho=10\Omega\cdot\text{cm}$		

Figure 1. Cross section view of CMOS chip on the silicon substrate

In our design, the square patch is realized on M1 metal layer and the loaded VNCAP is constructed from walls stacked with M2 to M6 metal wires and V1 to V5 vias on each edge of a square patch. A VNCAP loading AMC unit cell and AMC structure with 3x3 unit cells are shown in Figure 2.

The behavior of an AMC structure is determined by its physical dimensions. Hence, there are three parameters affecting its performance, namely, the patch width "a", the gap between two AMC unit cells "g", and the width of the wall "f". According to the equivalent LC lumped circuit model of the AMC [8], a wider patch width leads to a larger capacitance and increasing the gap width will decrease the value of the capacitance. The width of the stacked walls "f" has little effect on the AMC's reflection phase to be found by simulation, thus, the parameter "f" is equal to  $5\mu\text{m}$  for simulating fast.

Figure 3 shows the simulated reflection phase after being optimized. The VNCAP loading AMC unit cell has the dimensions  $(d+g) \times (d+g)$  of  $78\mu\text{m} \times 78\mu\text{m}$ . The width of the square patch, "a", is  $73\mu\text{m}$ , the gap between two AMC unit cells, "g", is  $5\mu\text{m}$ . The proposed AMC surface exhibits a reflection phase to be close to 0 at 61.5 GHz. The frequency bandwidth of AMC is between 53 and 70 GHz, at which the

reflection phase is within  $+90^\circ$  and  $-90^\circ$ . For the unlicensed 9-GHz working bandwidth from 57 to 66 GHz, the reflection phase is within  $+60^\circ$  and  $-60^\circ$

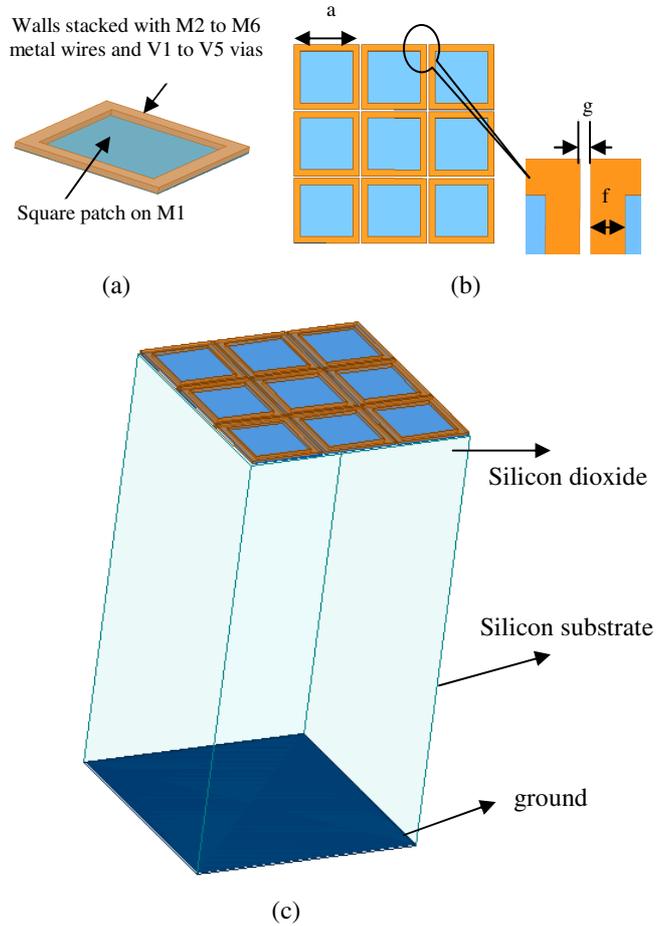


Figure 2. (a) Unit cell geometry of the proposed VNCAP loading AMC, (b) Top view of the AMC structure with 3x3 unit cells, (c) 3D view of the AMC structure with 3x3 unit cells

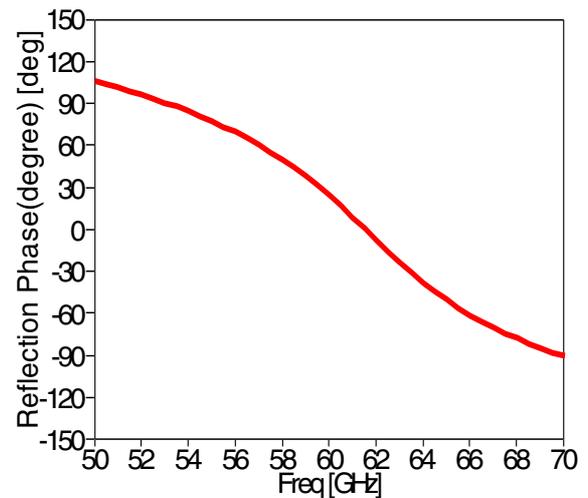


Figure 3. Simulated reflection phase of plane wave incident on AMC structure

### III. ANTENNA DESIGN OVER THE AMC

At first, the 60-GHz tab monopole on-chip antenna designed in previous work [9] is modified to be a U-shaped monopole on-chip antenna without AMC and the structure of the modified antenna is ultimately optimized using HFSS to be  $W = 1$  mm,  $W1 = 0.8$  mm,  $W2 = 0.2$  mm,  $L = 1.5$  mm,  $L1 = 1.06$  mm,  $L2 = 0.28$  mm,  $L3 = 0.56$  mm and  $L4 = 0.46$  mm. The proposed on-chip antenna is realized using terminal aluminum layer (LB layer) fed by  $50\Omega$  conductor-backed CPW line as described in [9]. The 3D view of the modified on-chip antenna structure without AMC is shown in Figure 4. The goal to adopt a U-shaped monopole antenna instead of a tab one is to reduce the mutual coupling between the AMC and monopole antenna after they are integrated while keeping the antenna performances almost the same.

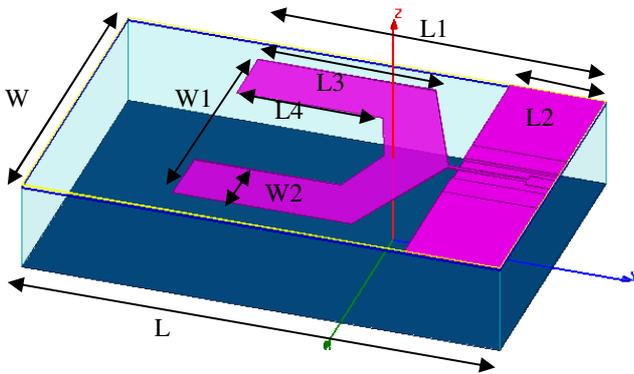


Figure 4. 3D view of the On-chip antenna structure without AMC

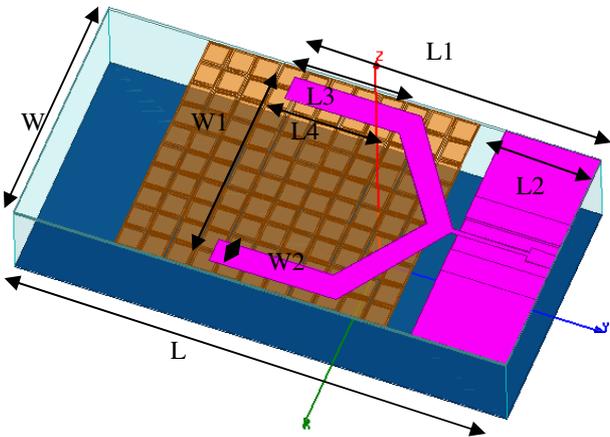


Figure 5. 3D view of the On-chip antenna structure with AMC

Then the modified antenna is put over the AMC surface and simulated together with AMC. The structure of the monopole on-chip antenna would be tuned because of the mutual coupling between the AMC plane and the antenna. In order to design a compact antenna without compromising performance, the optimization is performed to minimize the antenna size. As shown in Figure 5, the final optimized dimensions are  $W = 0.78$  mm,  $W1 = 0.7$  mm,  $W2 = 0.07$  mm,  $L = 1.55$  mm,  $L1 = 0.95$  mm,  $L2 = 0.28$  mm,  $L3 = 0.40$  mm

and  $L4 = 0.36$  mm. The width of the antenna had been narrowed to account for mutual coupling and the size of the entire structure was approximately 19.4% smaller.

### IV. SIMULATION RESULTS AND DISCUSSION

With the 3D configurations shown in Figure 4 and Figure 5 as the HFSS schemes for the U-shaped monopole on-chip antenna without AMC and with AMC, the simulated return loss, realized gain and radiation efficiency are plotted in Figure 6, Figure 7 and Figure 8 respectively. It can be seen that the return loss less than  $-15$  dB cover the band of 54-72 GHz for the antenna with AMC, but the return loss less than  $-15$  dB only covers from 54 to 67 GHz for the antenna without AMC. This indicates that the impedance bandwidth is improved while the antenna is mounted on AMC.

The realized gain of the U-shaped on-chip antenna over the novel AMC presented in Figure 7 is improved compared with the antenna without AMC. The maximum gain is 0.95 dBi at frequency 66 GHz, higher than that without AMC, whose maximum gain was only 0.14 dBi at frequency 63 GHz. The explanation for the improved gain is that the radiation efficiency is enhanced as shown in Figure 8. The simulated antenna radiation efficiency is between 41.6% and 50.8% within the frequency range from 57 GHz to 66 GHz. Obviously the simulated radiation efficiency with AMC is higher than that without AMC.

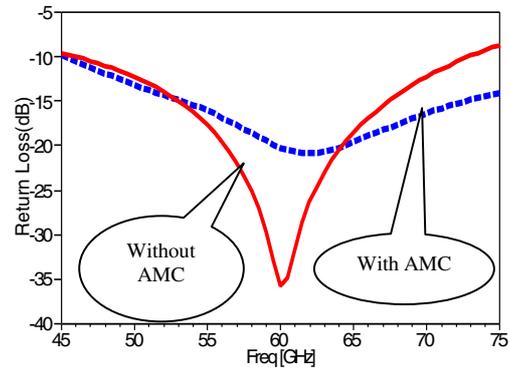


Figure 6. Simulated Return Loss Curve

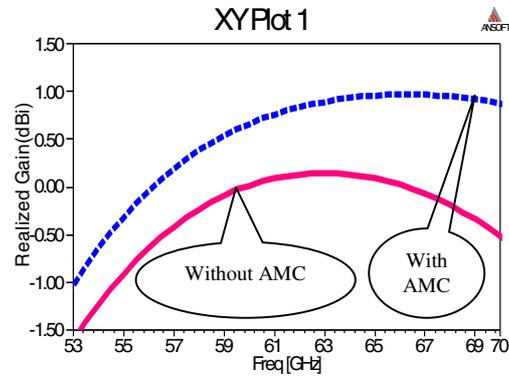


Figure 7. Simulated realized gain

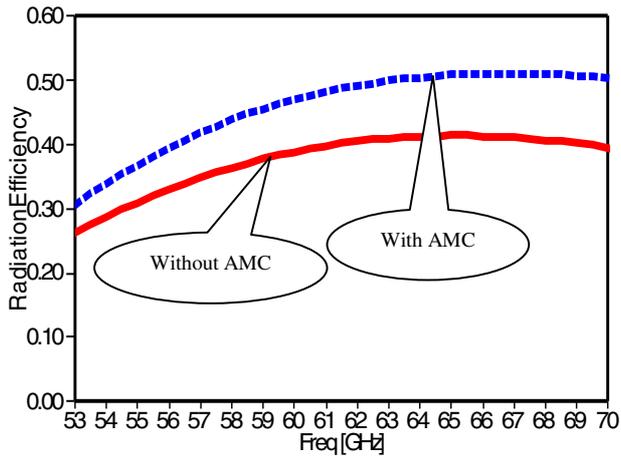


Figure 8. Simulated radiation efficiency

## V. CONCLUSION

In this paper, a compact and efficient 60-GHz U-shaped on-chip antenna mounted on a vertical natural capacitor (VNCAP) loading AMC that may be realized with the back-end-of-line process of standard 65 nm CMOS silicon Technology was presented. The size of the antenna including the novel AMC structure is  $1.55 \text{ mm} \times 0.78 \text{ mm} \times 0.28 \text{ mm}$ . Ansoft HFSS was used for design simulation centered at 61.5 GHz. The simulated results show that the U-shaped monopole on-chip antenna over the VNCAP loading AMC could achieve higher gain and radiation efficiency within the 60 GHz band. The return loss less than  $-15\text{dB}$  from 54 GHz to 72 GHz indicates a wider impedance bandwidth.

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