A CMOS Broadband Amplifier with Flatness Bandwidth for UWB Application  
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ABSTRACT
In this paper, a broadband distributed amplifier (DA) is presented. This circuit adopts two-stage cascode gain cell and m-derived matching section to enhance the gain and bandwidth performances. The series inductor placed at the inter-stage of the cascode cell can increase gain without any additional power consumption. A parallel resistor between the two-stage also enhances the gain flatness at low frequencies. The broadband DA is fabricated by a standard 0.18 \( \mu \text{m} \) CMOS process. The simulated results demonstrate that it achieves a power gain of around 10 dB, input and output return losses better than 8.3 and 8.56 dB, respectively. Isolation of this DA is better than 30 dB. The noise figure is around 5.23 dB.

INTRODUCTION
A distributed amplifier is commonly applied to high-speed data links, satellite communications, high-resolution imaging system, broadband optical communication, and ultra-wideband system. Thanks to the distributed architecture, it provides such performance by absorbing the parasitic capacitances of parallel gain stages into an artificial transmission line, which not only results in the gain flatness and uniformity, but also lets input/output match within the bandwidth of operation [1]. Although conventional DAs can achieve a broadband bandwidth, its gain is not high because of the additive gain mechanism.

In order to improve the gain of the DA, a cascade of inductively coupled common-source gain cells was proposed [2]. The DA uses a cascade gain cell to increase the gain and m-derive matching sections to reach input matching lower than -8 dB, and contains the gain 7.3±0.8 dB [3]. Besides, there are a lot of methods to improve the performance of DA. A CMOS DA with extended flat bandwidth and improved input matching by using gate lines and coupled inductors was be presented, and its input and output return losses are lower than 16 and 18 dB, respectively [4]. In [5] and [6], the DAs used four and five gain cells to achieve high gain and bandwidth flatness. In this paper, a two-stage cascode gain cell with a series inductor extends the bandwidth, and the parallel resistor between two stages enhances the gain flatness at low frequencies.

CIRCUIT DESIGN
DAs can achieve broadband bandwidth because of the distributed architecture. A conventional DA in Fig. 1 consists of an input and an output transmission lines coupled by the transconductances of the MOSFETs. The transmission lines are formed by using series inductors and gate-to-source capacitances of the transistors. In this topology, the input and output parasitic capacitances are absorbed in the distributed structures, which composed by these series inductors. Due to the distributed structure, the input and output signal can be not only separated obviously, but also enhance the isolation. The gain G of the conventional distributed amplifier has been analyzed in [2], [9], by
where $n$ is the number of the gain stages, $g_m$ is the transconductance of each gain cell, and $Z_{0g}$ and $Z_{0d}$ are the characteristic impedance of input line and output line, respectively. From equation (1), when the $Z_{0g}$ and $Z_{0d}$ are fixed to a certain value, the gain $G$ of DA is affected by $g_m$ and $n$.

\[
G = \frac{n^2 g_m^2 Z_{0g} Z_{0d}}{4}
\]  

(1)

Where $\theta_{rd}$ and $\theta_{rg}$ are real parts of the gate and drain line propagation constants, respectively. There is no limit on the number of stages in a DA with lossless artificial lines. However both gate and drain artificial lines are lossy in practice. Therefore, there is an optimum value for the number of stages, which is given by [4], as described in (2). Although the gain can be increased by number of stages before it reaches a maximum number, as given in [2] and [9], limited by the increasing losses of the artificial transmission lines, it results in larger die area and higher power consumption.

\[
N_{\text{opt}} = \ln \frac{\theta_{rd}}{\theta_{rg}}
\]

(2)

In this work, the CMOS DA was designed using two cascade gain cells, which provides high available gain, bandwidth, improves input-output isolation, and variable gain-control capability. The proposed DA uses $m$-derived sections [3] to achieve input matching, and the series-peaking inductor ($L_4$) in gain cell can extend the bandwidth without any power consumption [4]. The parallel resistor between two gain cells can enhance the gain flatness at low frequencies. The simulation gain versus different parallel resistances is shown in Fig. 3. It can see obviously that as the resistance becomes larger, the flat gain response is achieved at low frequencies. In this work, 36 ohm is chosen for the resistance to obtain a flat gain response. The $L_1$, $C_1$ and $C_2$ ($m$-derived matching sections) are used to implement the input matching network. And the output matching network is designed by a buffer amplifier and $L_3$. The resistors $R_b$ in the body of transistors $M_1$-$M_4$ are used to increase the overall gain in the circuit, shown in Fig. 4. The CMOS distributed amplifier design uses two stages to enhance the total gain with reasonable die area and small power consumption. Fig. 5 shows its microphotograph, and it consumes a chip area of 0.93 × 0.84 mm².
RESULTS

A DA was designed using a 0.18 μm 1P6M CMOS process. The CMOS DA chip will be tested via on-wafer probing using ground-signal-ground air probes. At the bias conditions of $V_1=1\,\text{V}$, $V_2=0.78\,\text{V}$, $V_3=1.5\,\text{V}$, $V_4=0.85\,\text{V}$ and $V_5=0.8\,\text{V}$, the bias current of each gain cell and buffer of the DA was 5.95 mA and 3.76 mA. The resistance of $R$ and $R_b$ are chosen 36 ohm and 5 kohm, which not only increase the total gain but also become flatness. Fig. 6 shows that the simulated power gain, the gain ($|S_{21}|$) is 10 dB with ripple 1 dB from 7 GHz to 19.5 GHz. The reverse isolation $|S_{12}|$ is -20 dB or better over the desired bandwidth. The input and output return losses are less than -8 dB in the entirely desired band. The noise figure is between 4.8 dB and 6.24 dB over the 7-19.5 GHz band, as shown in Fig. 5. And the Table I summarizes the performance of DAs in CMOS process. In Table I, it shows that this work features the lowest power consumption and the highest value of FOM.

CONCLUSION

A fully integrated broadband distributed amplifier has been designed, fabricated by using TSMC 0.18 μm CMOS process. The proposed amplifier consists of two-stage gain cell, which are cascode architecture to enhance the gain and bandwidth. In the circuit, the parallel resistance between two-stage is used to enhance the gain flatness at low frequencies, and the series inductor in one cell can extend the bandwidth without any additional power consumption. The simulation results show that the proposed DA is suitable for broadband communication applications.
REFERENCES


### TABLE I

**PERFORMANCE COMPARISON OF DISTRIBUTED AMPLIFIER IN A 0.18 μm CMOS PROCESS**

| Ref. | Bandwidth (GHz) | Gain (dB) | |S11| (dB) | |S22| (dB) | NF (dB) | P DC (mW) | Chip Area (mm²) | FOM | No. of Stages |
|------|-----------------|----------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| [2]  | 11              | 10       | <-20            | <-10            | 4.7             | 19.6            | 1.44            | 1.51            | 3               |                 |                 |
| [4]  | 16              | 10       | <-16            | <-18            | 3.6-4.9         | 21              | 1.19            | 2.3             | 4               |                 |                 |
| [5]  | 20              | 8        | <-10            | <-10            | 4.2-5.7         | 25.2            | 0.934           | 1.6             | 4               |                 |                 |
| [6]  | 25              | 9±1      | <-8.5           | <-8             | 3.8-4.5         | 158             | N.A.            | 0.5             | 5               |                 |                 |
| This work | 12.5         | 10.9     | <-8             | <-8             | 4.8-6.24        | 15.1            | 0.75            | 2.0             | 2               |                 |                 |

FOM[GHz / mW] = \frac{|S_{21}| * BW[GHz]}{(NF-1) * P_{DC}[mW]}

**REFERENCES**