A Novel charge pump architecture for driving CMOS active pixel reset

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Abstract

This paper presents a novel charge pump which overcomes the limitation of low image signal swing and long reset time in the four transistor CMOS active pixel image sensor. Unlike the conventional charge pumps in the literature, the output of the voltage doubler does not directly connected to the load. Alternatively, the high voltage is served as the power supply to a reference buffer. A high precision reference voltage is fed to the reference buffer. Thus, low voltage ripple is achieved with this architecture. In order to control the output voltage within the required range, a feedback loop is included. The simulation results show that with this architecture, the output of the charge pump is enhanced from 1.05V to 4.1V with ripple less than 2mV when driving a 764×524 CMOS image sensor.

1. Introduction

With the development of multi-media technology, CMOS image sensor has gained significant ground over the conventional charge-coupled devices (CCD) due to its high level integration, low-power operation and low cost [1]-[6]. As with the scaling down in integration process, the power supply decreases. This causes a notable loss of signal swing at the output of pixel [3], [6]. In order to overcome the signal swing loss, one wish to increase the voltage at the gate of reset transistor [3], [6]. As with those conventional charge pumps, the output is directly connected to the pixel reset terminal. This will cause large voltage ripple when the imager is used to high definition applications.

This paper presents a novel charge pump which consists of a time-interleaved voltage doubler, a reference buffer, a non-inverting clock generating module, a ring oscillator and a feedback loop. Output of the time-interleaved voltage doubler is served as the power supply to the reference buffer. The output of the reference buffer is then connected to the pixel reset terminal. The reset transistor driven by higher gate voltage level works in linear region thus it can accelerate the resetting process. With the proposed charge pump, the signal swing at the output of pixel is also enlarged. The post-layout simulation results show that the proposed charge pump can raise the reset signal from 3.3V to 4.1V with voltage ripple less than 2mV.

The rest of the paper is organized as follows. The second section describes the details of the proposed charge pump architecture. Section III gives the simulation results. The last section concludes the paper.

2. Proposed charge pump architecture

The architecture of the proposed charge pump is shown in Figure 1.

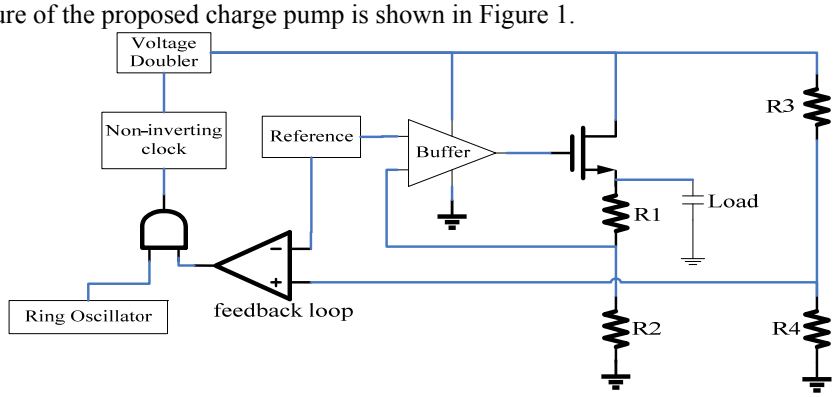

Figure 1 ARCHITECTURE OF THE PROPOSED CHARGE PUMP

Unlike the conventional charge pump used in image sensor, the time-interleaved voltage doubler does not directly connect to the pixel reset terminal. In the presented one, the voltage doubler is served as the power supply to the reference buffer which loads the pixels.

By this way, the output ripple seen by the pixels is the attenuated one. The power supply rejection ratio of the reference buffer is the attenuation factor. Since the power supply rejection ratio can be with the same order of

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half hundred dBs. Thus, a small voltage ripple is achieved at the reference buffer. This will in turn makes the design of voltage doubler easy.

The working principle of the proposed charge pump is as follows: voltage doubler increases the voltage from 3.3V to 4.5V. The output of voltage doubler is used as the power supply to the reference buffer. Since non-inverting clock is required to make the voltage doubler work properly, a non-inverting clock generating circuit and a ring oscillator are included in the design. Because over high driving voltage will damage the transistors or cause reliability problem, a feedback loop is used to control the output voltage of voltage doubler to be under 4.5V. Thus a voltage of 4.1V is given to the reset terminal of the pixel.

The following section gives the detailed circuit of the proposed charge pump.

2.1 Time-interleaved voltage doubler

In this paper, a time-interleaved voltage doubler is used to reduce the output voltage. The schematic is shown in Figure 2.

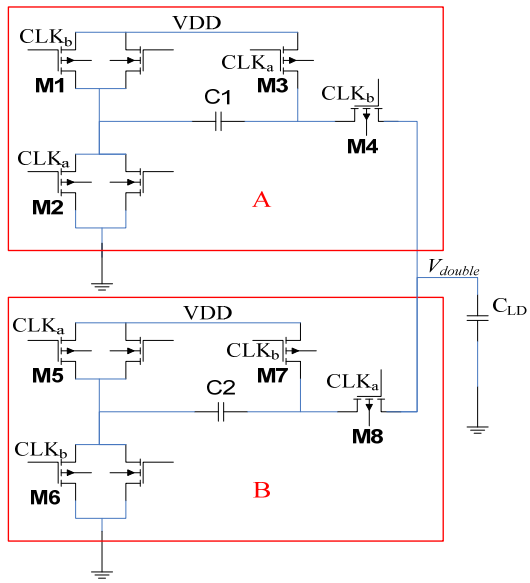

Figure 2 TIME-INTERLEAVED VOLTAGE DOUBLER

The time-interleaved voltage doubler is consisted of two identical voltage doublers which operate in complementary mode. Upper part of the schematic, namely switch M1, M2,M3,M4 and capacitor C1 consist of one voltage doubler denoted as A. Lower part of the schematic, namely switch M5,M6,M7,M8 and capacitor C2 consists of the other voltage doubler denoted as B. There are two working stages of every individual voltage doubler, they are charging stage and output stage.

The working principle is the same for both voltage doubler A and B. In the following, the working principle of voltage doubler A is explained. Their two stages are:

Charging stage: when CLKa is high, CLK_b is low，switches M2 and M3 turns on，switches M1 and M4 are off. Thus C1 is charged by the power supply. At the end of this stage, the voltage at the right plate of C1 is VDD;
Output stage: when CLKa is low, CLKb is high，switches M2 and M3 turns off，switches M1 and M4 are on. The left plate of C1 is connected to power supply. Due the fact that voltage across the capacitor can not jump instantaneously, the voltage on the right plate of C1 is 2VDD. By the same time, the voltage doubler charging the output load C_{LD}.

If the output is directly connected to pixel reset terminal, such simple voltage doubler can not meet the requirement even though adopting the time-interleaved technique. In order to further reduce the ripple seen by the reset terminal of pixel, a reference buffer which loads the pixel directly is used.

CLKa and CLKb in Figure 2 are non-inverting clocks which guarantee that M1 and M2 are not in the on state at the same time. CLKa and CLKb are generated with the non-overlapping clock generating circuit. The input clock of the non-inverting clock generation circuit is given by a ring oscillator which is made of an inverter chain. The inverter chain has seven inverters whose power supply is controlled by a current source. Thus, the ring oscillator's frequency can be turned by the current.

Avoiding the time-interleaved voltage doubler jumps to a high voltage, a feedback loop is needed. A scaled version of the output of voltage doubler is compared with a reference voltage which is 1.15V. The

compared result is used to control the clock of voltage doubler. If the voltage at the voltage doubler is higher than 4.5V, then the control signal disables the clock signal.

2.2 Reference buffer

The schematic of the reference buffer is shown in Figure 3. It consists of a folded cascode amplifier, a common source amplifier and a resistor ladder. The power supply of the reference buffer is the output of time-interleaved voltage doubler denoted as V_{double} in the schematic. Output of the reference is fed to the pixels. The minus positive terminal of the reference buffer is connected to a reference voltage which is 1.0V. With this reference buffer, an amplified version of the reference which is 4Vref is fed to the pixels.

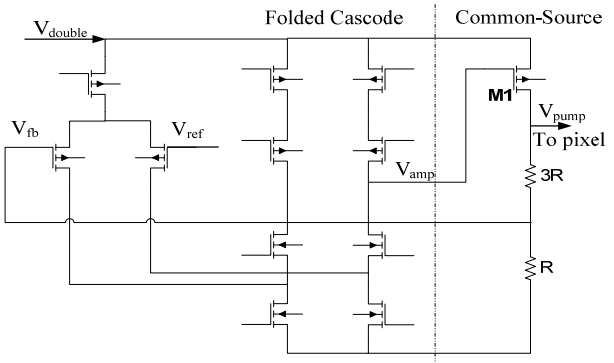

Figure 3 REFERENCE BUFFER

Assuming the ripple of the time-interleaved voltage doubler is ΔV_{double}, neglecting the second order effect of M1, we can get the ripple voltage at the output of the amplifier

$$\Delta V_{amp} = \Delta V_{double} \tag{1}$$

Assuming the open loop gain of the amplifier is A_{fc}, and then the voltage fluctuation at the minus terminal of reference buffer is

$$\Delta V_{fb} = \frac{\Delta V_{amp}}{A_{fc}} = \frac{\Delta V_{double}}{A_{fc}} \tag{2}$$

Since a resistor ladder is added to amplify the reference voltage, then the ripple voltage at the output can be expressed as

$$\Delta V_{pump} = 4 \times \Delta V_{fb} = \frac{4 \times \Delta V_{double}}{A_{fc}} \tag{3}$$

From the above equation, we can see that voltage doubler's ripple is greatly reduced by the PSRR of the fold-cascoded amplifier. In practice, the ripple voltage can inject to the output through M1 considering the higher order effect. With carefully design, we can reduce the higher order effect greatly. Thus, with the novel architecture, the ripple voltage is small enough to meet the requirements of the pixel even we use such simple voltage doubler.

3. Simulation Results

This section gives the simulation results of the proposed charge pump. The charge pump system is designed in Tower Semiconductor Ltd. 0.18um CMOS process. The charge pump is successfully embedded in a CMOS image sensor chip with 764×524 pixel.

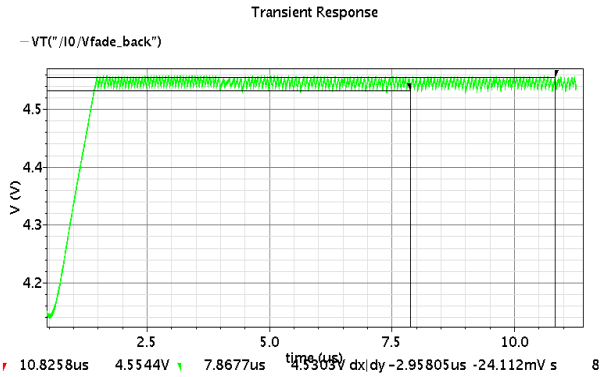

Figure 4 OUTPUT OF TIME-INTERLEAVED VOLTAGE DOUBLER

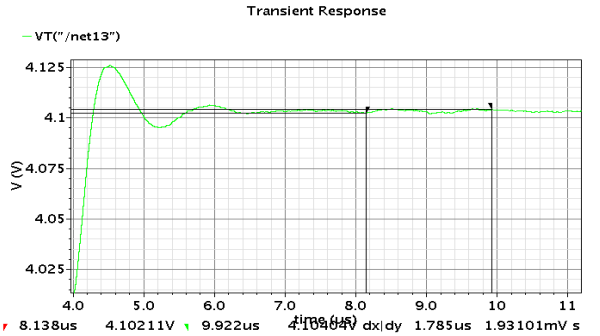

Figure 5 OUTPUT VOLTAGE OF REFERENCE BUFFER

Figure 4 shows the output voltage of the time-interleaved voltage doubler while Figure 5 shows the voltage connected to the reset terminal. It can be seen from the Figure 4 that the voltage is about 4.5V with its ripple about 24mV. The voltage supplied to reset terminal of pixel is about 4.1V with its ripple 1.93mV.

From the Figure 4 and Figure 5, we can see that the proposed charge pump generates the reset signal with extremely good ripple performance even with simple voltage doubler.

4. Conclusion

A new charge pump circuit for four transistor pixel is proposed in this paper. Unlike conventional charge pump, the proposed one uses a reference buffer to directly load the pixel array. With this architecture, a low voltage ripple is achieved even with a simple time-interleaved voltage doubler. A voltage feedback loop is used to force the voltage within the required range. With the help of the proposed charge pump, pixel signal swing range is enlarged.

5. References

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