A two-stage low-power amplifier with switch-capacitor common-mode feedback circuits

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Abstract

A low-power amplifier is designed to improve the performances of ADCs. The two-stage construction is adopted to provide bigger gain and wider swing at a power supply lower than 3.3V. Besides, the differential architecture is adopted to double the output swing while suppressing common noises. Special common-mode feedback circuits are designed to stable the common-mode outputs of the first and second stages but not to degenerate the output swing. A private switch is designed for the common-mode feedback circuits to eliminate the charge injection effect on the common-mode signals. The measurement results show that the ADC using the proposed amplifier has a SNR which is 4dB better than the ADC without the proposed amplifier.

1. Introduction

Amplifiers as basic block for ADCs are very important [1-5]; they decide the performance of the whole ADC. As the communication field demands ADCs with higher performance, amplifiers with bigger gain, wider output swing are required. Meanwhile, as the improvement of semiconductor manufactural process, the lower power supply voltage is adopted. So, how to design a amplifier with big gain and wide swing while working under 3.3V or lower power supply is a puzzle for analog/mixed signal integrated circuit engineers. In this paper, a novel two-stage amplifier is designed, which uses two-stage construction to provide enough gain for 14 or higher bit ADC while providing adequate output swing. As we know, the differential architecture has better performances than its single-end counterpart, so the differential architecture is adopted in the design of the amplifier. For differential amplifier, common-mode feedback circuits have to be added to provide stable common-mode output signal. So, how to design a common-mode feedback circuit to stable the common-mode output while not to degenerate the swing is another puzzle faced by nowadays engineers.

2. Circuit

As shown in figure 1, the proposed amplifier consists of two stages. The first stage is a full differential cascode amplifier which consist of a differential pairs of NMOS transistors N1 and N2, tail current source N3, a pair of common gate NMOS transistors N4 and N5, a pair of common gate PMOS transistors PMOS transistors P1 and P2, a pair of common source PMOS transistors P3 and P4, and two auxiliary amplifiers A1 and A2, which are used to boost the gain of the amplifier. The main purpose of the first stage is to provide gain for the whole circuit. The second stage is a general full differential amplifier with PMOS transistors as active loads. Besides the two-stage amplifier, shown in figure 1 are the input capacitors C_is, feedback capacitors C_os, and several sampling and hold switches. The gain of the first stage can be written as

$$G_1 = g_{mN1}(r_{oN1}A_2 g_{mN4} r_{oN4} \,||\, r_{op3}A_1 g_{mp1} r_{op1}) \tag{1}$$

where g_{mN1}, g_{mN4}, and $g_{mp1}$is the transconductance of transistors P1, respectively, r_{oN1}, r_{oN4}, and r_{op3} are the output impedance of transistors N1, N4 and P3, respectively, and A_1 and A_2 are the gain of the auxiliary amplifier A_1 and A_2. The capacitors C_1 and C_2 function as miller compensating capacitors. Capacitors C_3 and C_4 work with switches S_1 and S_2 as the common feedback circuit for the first stage, which decides the output common signal level of the first stage.

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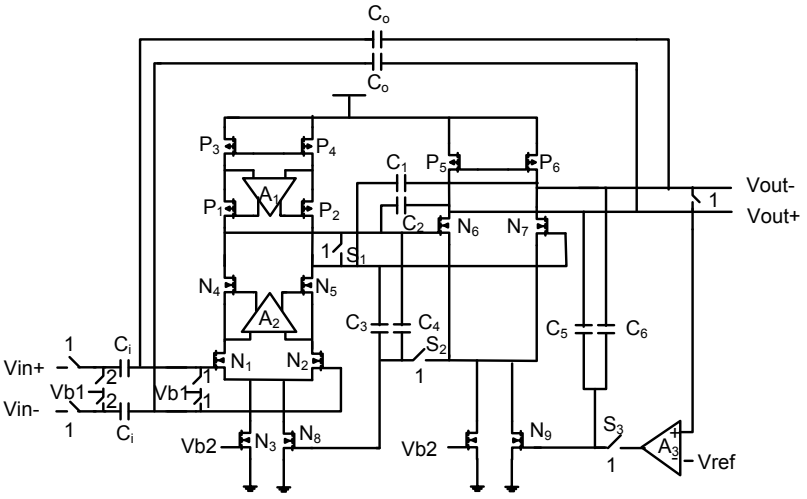

Figure 1. The circuit of the proposed two-stage amplifier

At the sampling phase all switches labeled with 1 is open and the two-stage amplifier works at a reset stage, at which the inputs and outputs of the first and second stages are all shorted together. A common feedback loop is formed from the outputs of the first stage to the common source of NMOS transistors N_6 and N_7, and to the gate of the NMOS transistor N_8, and back to the outputs of the first stage. It is a negative feedback loop because the gain from the gate to the outputs of the first stage is negative. At the sampling phase, the common output signal of the first stage is

$$V_{1st\_common\_s} = V_{gs8} + V_{gs6} \tag{2}$$

where V_{gs8} and V_{gs6} are the gate-source voltage of NMOS transistors N_6 and N_8, respectively. Assuming, C_3=C_4, The charges sampled at node D is

$$Q_1 = -2C_3 * V_{gs6} \tag{3}$$

At the holding phase, the switch S2 is disconnected and the charges sampled at the gate of NMOS transistor N_8 is held, so the voltage at the gate of N8 is

$$V_{gs8} = V_{1st\_common\_h} - V_{gs6} \tag{4}$$

where $V_{1st\_common\_h}$ is the common output signal of the first stage at the holding phase. From equation (4), we get

$$V_{1st\_common\_h} = V_{gs8} + V_{gs6} \tag{5}$$

which is the same as (2). So the common level of the first stage keeps the same at the different working steps. The second stage of the two-stage amplifier is used to broaden the output swing meanwhile providing some gain. The gain of the second stage is

$$G_2 = g_{mN6}(r_{oN6} \,||\, r_{op5}) \tag{6}$$

where g_{mN6} is the transconductance of NMOS transistor N6, and r_{oN6} and r_{op5} are the output impedance of transistors N_6 and P_5, respectively. The whole gain is the product of the gains of the two stages, which is equal to G_1G_2. The capacitors C_5 and C_6, switch S_3, amplifier A_3 and NMOS transistor N_9 constitutes the common feed circuit for the second stage. At the sampling phase, all switches labeled 1 are closed. The loop from the outputs of the second stage to the output of the amplifier A_3, and back to the outputs of the second stage forms the common feedback circuit. For the loop working properly, the feedback has to be negative. In order to achieve that, the outputs (Vout+ and Vout-) are connected to the positive terminal of the amplifier A_3, because the gain from the gate of N_9 to the outputs is negative.

Besides, because the gain from the gate of N_9 is large, the auxiliary amplifier A_3 doesn't need a big gain. Because of the negative feedback loop, the common mode output of the second stage is equal to V_{ref}. Assuming C_5=C_6, the charges sampled on the gate of N9 are

$$Q_2 = 2C_5(V_{gs9} - V_{ref}) \tag{7}$$

where V_{gs9} is the gate-source voltage of NMOS transistor N_9. At holding phase, all switches labeled 1 are disconnected including S_3. The charges on the gate of N_9 are kept, so the voltage this node is

$$V_{gs9} = \frac{2C_5(V_{gs9} - V_{ref})}{2C_5} + V_{2nd\_common\_h} \tag{8}$$

where $V_{2nd\_common\_h}$ is the output common signal of the second stage at the holding phase. Reducing (8), we get

$$V_{2nd\_common\_h} = V_{ref} \tag{9}$$

So the common mode output kept unchanged at the sampling and holding phase. From the analysis above, we find that the charges stored at the gates of NMOS transistors N_8 and N_9 are very important, because they decides the common mode output at the holding phase. In order to reduce the effect of charge injection, we design a new type of switch for S_2 and S_3 as shown in figure 2.

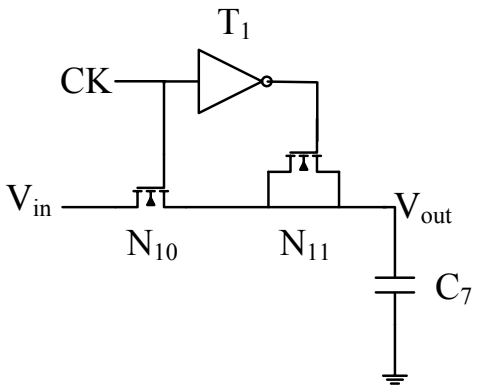

Figure 2. New type of switch for eliminating the charge injection effect

Capacitor C_7 is used to model the gate capacitor of NMOS transistor N_8 or N_9. The channel size of N_{11} is half that of N_{10}, so when the clock signal CK falls from high to low level, half the channel charges is injected onto capacitor C_7. Meanwhile, the output of the inverter T_1 rises from low to high level, NMOS transistor N_{11} is turned on, and the conductance channel formed under N_{11}, which absorbs the charges injected onto C_7, canceling the charge injection effect of N_{10}.

3. Measuremenet

Shown in figure 3 is the layout of the proposed amplifier and the spectrum of the proposed amplifier, we find that the SNR and SFDR are 79dB and 84dB. It is now integrated into a pipeline ADC to improve its performances. The pipeline ADC has been manufactured in a foundry. Shown in table 1 are the measurement results compared to a pipeline ADC without the proposed amplifier.

4. Conclusion

The simulation shows that the proposed amplifier can work under a power supply as low as 2V, while consuming only 45mW. The DC gain can achieve 90dB with a maximal output swing of $2V_{p\text{-}p}$. The measurement

results show that the ADC using the proposed amplifier has a SNR 4dB better than the ADC without the proposed amplifier. Other performances of the ADC are improved too because of the adoption of the proposed amplifier.

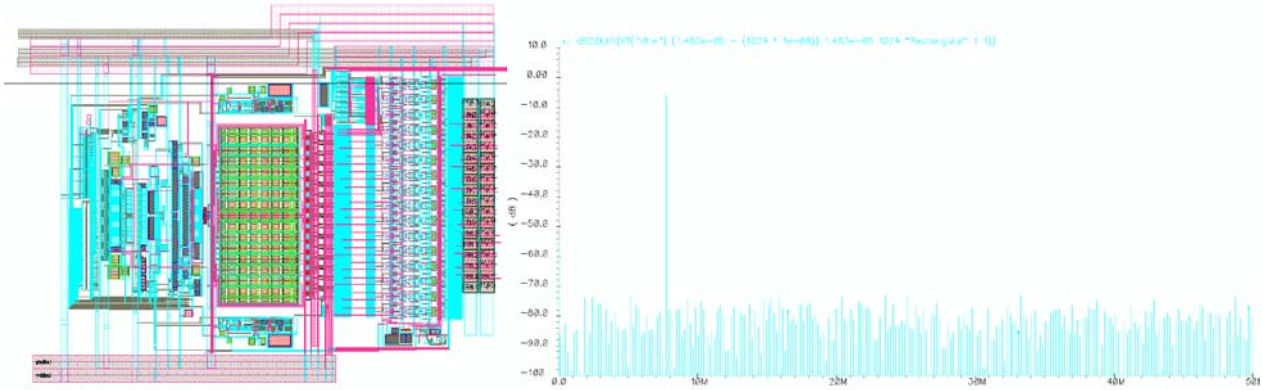

Figure 3. The layout of the proposed amplifier and the spectrum of the proposed amplifier

Table 1. The measurement results of the ADC

performances	ADC using the proposed amplifier	ADC not using the proposed amplifier
SNR	79dB	75dB
SFDR	85dB	80dB
INL	0.6LSB	1LSB
DNL	0.5LSB	0.9LSB
Maximal sampling rate	200MHz	190MHz
Power consumption	300mW	400mW

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