An integrated analog switch for multi-channel ADC

Hu Rongbin[1], Zhengping Zhang[2], and Yuxin Wang[1]*

[1]Science and Technology on Analog Integrated Circuit Laboratory, Chongqing 400060, China,
hurongbin2000@126.com, wangyuxin@126.com

[2]No.24 Research Institute, China Electronics Technology Group Corporation, Chongqing 400060, China,
zhangzhengping@126.com

Abstract

A new analog switch is introduced, which can be used in multi-channel ADC to ease channel selection. Because of special structure and circuit techniques being used, the proposed analog switch has extremely broad bandwidth and excellent linearity when working in passing state. Besides, it can isolate the incoming signal from the inside circuits perfectly when working at disconnecting state. The two-channel 8-bit ADC integrating the proposed analog switch [1] can sample an analog signal up to 1.5GHz with a sampling rate greater than 2GHz. The measurement results shown that the ADC achieves 0.3LSB DNL, 0.3LSB INL, 7.32 ENOB at 484 MHz input.

1. Introduction

Analog switches are often placed in the front of analog/mixed-signal integrated circuits (ICs) to configure several input signals and multi channels. One of the most important applications of analog switches is used in multi-channel ADC to allocate the incoming signals to the multi channels [2-4]. One of the typical applications is shown in figure 1, where four analog switches allocate two incoming signals to two ADCs. There are four kinds of configuration: IN_1 to ADC1, IN_2 to ADC2; IN_1 to ADC2, IN_2 to ADC1; IN_1 to ADC1, IN_1 to ADC2; IN_2 to ADC1, IN_2 to ADC2.

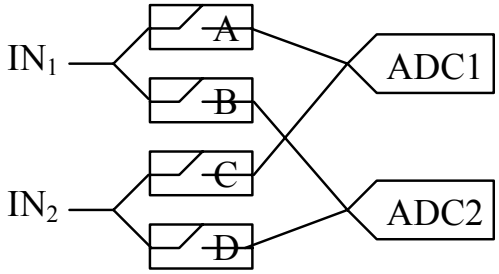

Figure 1. One typical application of analog switch

To realize IN_1 to ADC1 and IN_2 to ADC2, switches A and D are closed, while switches B and C are open. To realize IN_1 to ADC2 and IN_2 to ADC1, switches B and C are closed, while switches A and D are open. To realize IN_1 to ADC1 and IN_1 to ADC2, switches A and B are closed, while switches C and D are open. To realize IN_2 to ADC1 and IN_2 to ADC2, switches C and D are closed, while switches A and B are open.

For all the application, the analog switch must have excellent linearity and broad bandwidth when working at passing state with perfect isolation when working at disconnecting state. In this paper, a new novel analog switch implemented in SiGe BiCMOS process is introduced. Because of special structure and circuit techniques being used, the proposed analog switch has extremely broad bandwidth and excellent linearity when working in passing state. Besides, it can isolate the incoming signal from the inside circuits perfectly when working at disconnecting state.

2. Structure

In order to maximize the linearity, the full differential construction is adopted as shown in figure 2, where the whole block diagram is symmetric about the central vertical line [5,6]. The whole structure consists of two symmetric input buffers B1 and B2, two inter-stage switches S1 and S2, a bias circuit BIA, a control cell C, and output buffer O.

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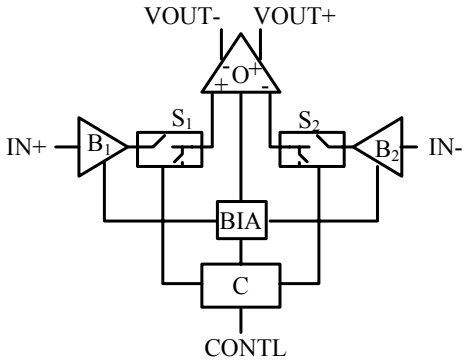

Figure 2. The block diagram of the analog switch

The incoming differential signals IN+ and IN- are first buffered by B1 and B2, and then passed through switches S1 and S2 to drive the output buffer O. The bias circuit provides bias for all the other cells. The control cell C controls the on-off states of the inter-stage switches and powers down the whole circuit when the switches are closed.

3. Circuit

The transistor-level circuit of the whole analog switch is shown in figure 3. The inter-stage switch S_1 in figure 2 is realized by PMOS P_1, NMOS N_9 and N_{10}, while S_1 is realized by PMOS P_2, NMOS N_{11} and N_{12}. The control cell C in figure 2 is implemented by inverters T_1 and T_2. The circuit composed of PMOS P_3, P_4, NMOS N_{13}, and resistor R_5 is used to bias the input buffers B_1 and B_2.

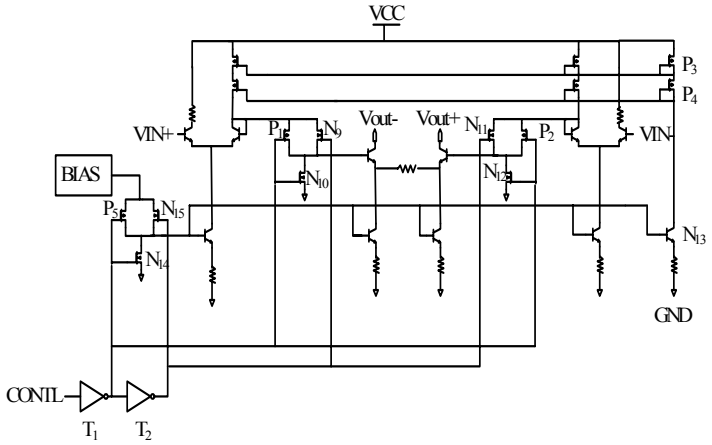

Figure 3. the transistor-level circuit of the proposed analog switch

When force a high level on the controlling signal CONTL, inter-stage switches S_1 and S_2 are turned on. The outputs of the input buffer B_1 and B_2 are connected to the inputs of the OTA. Meanwhile P_5 is turned on, with N_{15} and N_{14} off. BIAS is connected to the cells which need bias current or voltage. As a result, when CONTL is high level, the analog switch is on. When CONTL is low level, inter-stage switches S_1 and S_2 disconnect the inputs of the OTA from the outputs of the input buffers, and pull the inputs of the OTA down to GND. And the transistors P_5, N_{15}, and N_{14} disconnect BIAS from the cells and pull the bases of the bias NPN transistors to down GND to shut down every power consuming cells.

As we see, when the analog switch is on, only fast SiGe NPN transistors are on the signal path, so the bandwidth is very broad. The bandwidth of the analog switch can be calculated as below:

$$\omega_{bandwidth} = \frac{C_p}{g_m} \tag{1}$$

where g_m is the transconductance of the SiGe NPN transistors on the signal path and C_p is the parasitic capacitance at the inputs of the OTA. The gain of the analog switch can be expressed as:

$$G_{ain} = \frac{A}{1+A}\frac{2R_C}{R_E} \tag{2}$$

where A is the loop gain of the input buffer, R_C is the resistance of the resistors connected to the outputs of the OTA, and R_E is resistance of the degenerating resistor connected to the emitters of the input transistors of the OTA. Generally, the gain of the analog switch is not important, so G_{ain} is usually set to one. Because of the adoption of unit-gain feedback amplifier in input buffers and the usage of emitter degenerating resistor, the analog switch will have excellent linearity.

When the analog switch is off, the outputs of the input buffers are disconnected from the inputs of the OTA. Besides, the inputs of the OTA are pulled down to GND, so the outputs of the OTA are completely uninfluenced by the incoming signals.

4. Application

Currently the proposed analog switch has been used in a two channel ADC to easy channel selection. The microphotograph of the ADC with the proposed analog switches is shown in figure 4.

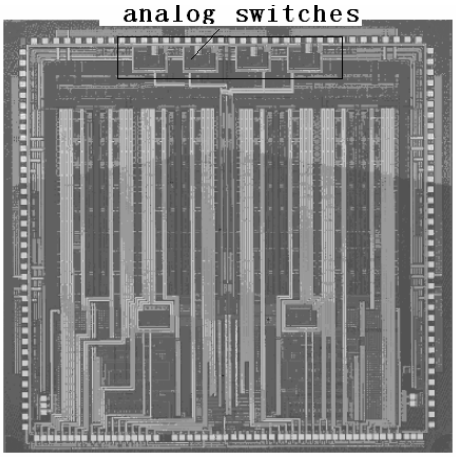

Figure 4. Microphotograph of the ADC with proposed analog switches

Because of the adoption of the analog switches, the two-channel ADC can work at either two-channel Q&I mode or one-channel time-interleaving mode [7]. Especial at time-interleaving mode, the sampling rate is improved by two times compared to the one-channel mode.

5. Measurement

The ADC incorporating the proposed analog switch is realized in a 0.35um BiCMOS process. The measurement shows that the ADC can sample an analog signal up to 1.5GHz with a sampling rate greater than 2GHz. With an input bandwidth of 484MHz and sampling rate of 2GHz, the ADC achieves 0.3LSB DNL, 0.3LSB INL, 52dB SFDR, 45.8dB SNR and 7.32 ENOB as shown in figure 5, 6.

6. Conclusion

The successful application of the analog switch in a two-channel ADC proves that the analog switch has excellent linearity, broad bandwidth and perfect isolation ability. It can be used in high performance analog/mixed-signal ICs such as ADC, DAC, et al.

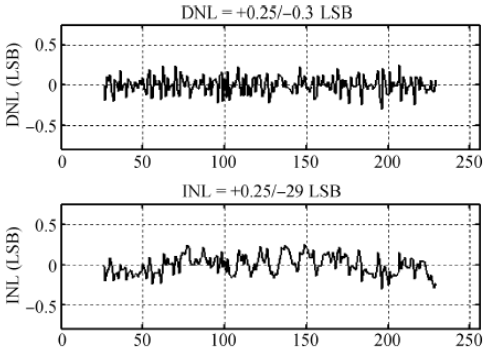

Figure 5. The DNL and INL measurement

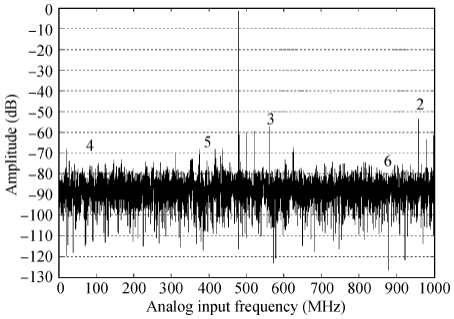

Figure 6. The SFDR measurement

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