Experimental Investigation and Electro-Thermal-Stress Modeling of GaAs and LDMOS FET under Conductive Electromagnetic Pulse (EMP)

Liang Zhou[1], Wei-Feng Zhou[1], Zhang Cheng[1], Liang Lin[1], Wen-Yan Yin[1,2], and Jun-Fa Mao[1]*

[1] Center for Microwave and RF Technologies (CMRFT), Key Laboratory of Ministry of Education of Design and Electromagnetic Compatibility of High-Speed Electronic Systems, Shanghai Jiao Tong University, Shanghai, 200240 CHINA, E-mail: liangzhou@sjtu.edu.cn

[2] Center for Optics and EM Research, State Key Lab of MOI, Zhejiang University, Hangzhou 310058, CHINA

Abstract

Investigation on conductive electromagnetic pulse (EMP) effects on performance degradation and breakdown of GaAs MESFET and LDMOS FET-based power amplifiers (PA) are performed in this paper. A special measurement system is built, which consists of an adjustable EMP source, one controller, couplers, limiters, attenuators, one four-channel oscilloscope, and DUT. The PAs performance degradation and their breakdown areas are observed and analyzed by using electro-thermal-stress models for the injected EMP with different widths. The thermal and stress results explain the experimental phenomena well and will be very useful for understanding the interaction mechanisms of real radio frequency power applications in a complex electromagnetic environment.

1. Introduction

In the past a few years, special attention has been focused on intentional electromagnetic interference (IEMI) effects on some communication systems [1], where low noise amplifiers (LNA) and power amplifiers (PA) can be easily disrupted and even physical damaged. Actually, all GaAs-built MESFETs and LDMOS FETs are very sensitive to the variation of the input electromagnetic signal where the degradation and breakdown process taken place in them is very complex to be solved. Under such circumstances, experiment-oriented study will be one directive and efficient way for fast characterizing breakdown field strengths, maximum current carrying densities or peak power handling capabilities of most active devices or components. On the other hand, the electro-thermal-stress (E-T-S) multi-field interactions of semiconductor devices [2] often depend on the device structure, EMP pulse widths, and repetition frequencies, which are not yet resolved. For example, stress effects are often observed in the experiments because EMP pulses generate a lot of heat in the semiconducting region, and the heat is distributed both to the bulk and the interconnection parts of the device. This can result in stress failure of the interconnection parts of the semiconductor device.

2. Measurement Setup

Figures 1 (a) and (b) show the measurement setup for investigating on performance degradation and breakdown of the GaAs MESFET and LDMOS FET-based PA caused by an injected EMP. It mainly consists of one EMP source, one controller, three limiters, two 30-dB couplers, three 10 to 30-dB attenuators, and one four-channel oscilloscope DPO7104. Figure 1 (c) shows one typical EMP signal shape in the time domain, which is important for characterizing its effect on the performance degradation of PAs. The total pulse width is 30ns and it can be adjusted up to 10ms. Its rise or fall time is about several nano seconds. Its amplitude can also be adjusted depending on the DUT and our interest.

In Fig.1(a), the controller is used to control the pulse width and the Pulse-Recurrence-Frequency (PRF) of the EMP source. The step attenuators are manually changed to increase the EMP amplitude gradually. One reference signal (0 dBm) from an Anrisu signal generator is also injected into the PA through one of directional couplers to monitor and compare the gain of the tested PA before and after the EMP injection each time. The power failure threshold of the GaAs MESFET PA is then recorded, when a sharp current peak emerges, its gain is decreased rapidly. This indicates that the DUT is destroyed. Here, the Pulse-Recurrence-Frequency (PRF) of the injected EMP is set to be 50Hz for our measurement.

3. MEASUREMENT RESULTS

Figures 2 (a) and (b) show the measured magnitudes of S_{21}-parameters of the GaAs MESFET and LDMOS FET PA for different EMP widths. The GaAs MESFET-based PA gain is about 30dB at the operating frequency

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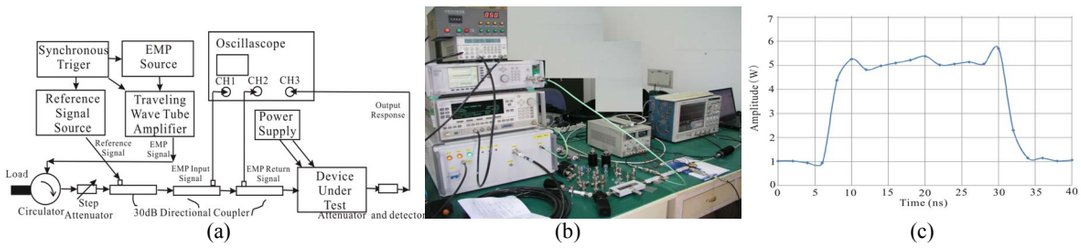
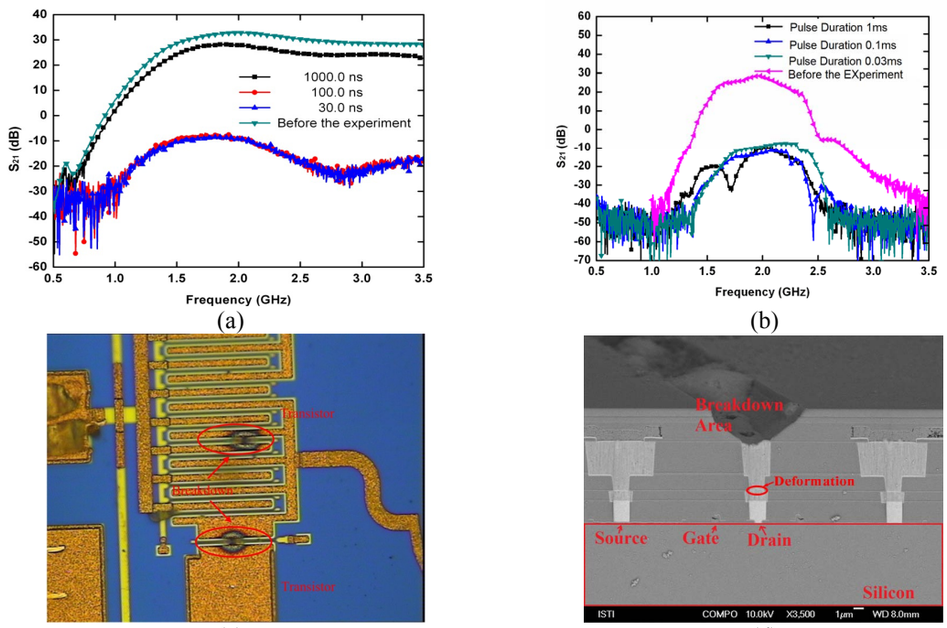
f = 2GHz before the EMP signal is injected. As the EMP width is increased from 30 to 100 and 1000.0ns, it is evident that the PAs performance are degraded significantly, and finally, they are electro-thermal broken down. Fig.2(c) and (d) shows the breakdown regions of the first-stage GaAs MESFET and LDMOS FET, respectively.



(a) (b) (c)

Fig.1. (a) and (b) Measurement system for studying on EMP effects on the DUT, (c) Single EMP waveform used for injecting into the DUT.



(a) (b)

(c) (d)

Figures 2 the measured magnitudes of S21-parameters of (a) the GaAs MESFET and (b) LDMOS FET PA for different EMP widths. breakdown regions of (c) the first-stage GaAs MESFET and (d) LDMOS FET

4. Numerical Calculations and Discussion

The breakdown of GaAs MESFET and LDMOS FET -based PA under an EMP impact is mainly caused by thermal effects as the duration time of the injected pulse is long. The analysis of thermal failure can be carried out based on the work reported by Dwyer *et al* [3], where the heat source is assumed to be a 3-D one. To simplify the thermal analysis here, the heat source can be reduced to be the 2-D one characterized by a ×b (μm^2) [4]. Under such circumstances, the failure power density of the FETS can be estimated.

In our analysis, the ambient temperature is chosen to be T_0 = 300 K, the thermal breakdown temperature of the FETS is represented by T_{cri}, λ is the GaAs or Silicon thermal conductivity (W/cm•K) , ρ is the mass density (g/cm^3), C_P is the specific heat capacity (J/g•K), $D = \lambda/\rho C_P$ is the thermal diffusivity (cm^2/s), and P_{fail} is the failure power per unit area of heat source.

For an infinitely thin rectangular heat source of a × b (μm^2), the temperature gradient in the rectangular region changes in both directions until an thermal equilibrium is reached in the direction of its shorter size (b), beyond which temperature changes in the other direction of its longer size (a). The time required for establishing their thermal equilibriums in both directions are determined by [4]:

$$t_a = \frac{a^2}{4\pi D}, \quad t_b = \frac{b^2}{4\pi D} \tag{1a, b}$$

where a > b. The failure power (P_0) depends on the time scale with respect to two diffusion time t_a and t_b [10], and

$$P_{R_I} = \frac{\lambda \pi T_{cri}}{\sqrt{4\pi D t}} \text{ when } t \le t_b \quad (2a), \qquad P_{R_{II}} = \frac{2\lambda\pi(T_{cri} - T_0)}{b[\ln(t/t_b) + 2]} \text{ When } t_b \le t \le t_a \quad (2b)$$

$$\text{And } P_{R_{III}} = \frac{\lambda\pi(T_{cri} - T_0)}{b[\ln(a/b) + 2 - \sqrt{t_a/t}]} \text{ When } t \geqslant t_a, \quad (2c)$$

Thus, it can be seen that there are three distinct time domains observed in the relationship of power versus time. It is possible that, depending on the area and layout aspect ratio of the device. For the LDMOS FET a = 362 µm, and b = 182 µm. Therefore, t_a and t_b are estimated to be 0.2ms and 50µs by using equation 1, indicating that region II dominates the relationship of power versus time from the time of 50 µs to 0.2 ms, and region III dominates the time beyond 0.2ms.

Fig.3 shows the three regimes which plot by using equations (2a) – (2c). The first regime (P_{RI}) dominates the time below t_b = 50 µs, where the measured the power to failure data with pulse duration 30 µs is located in this regime. The second regime (P_{RII}) dominates the time from t_b to t_a, the measured the power to failure data with pulse duration 0.1 ms is in this regime. The third regime (P_{RIII}) dominates the time from ta, where the measured the power to failure data with pulse duration 1 ms are located in this regime. By fitting the measured data to equations (2a) – (2c), we will have the breakdown temperature parameter (T_{cri} = 605 K) of the LDMOS FET. The Simple $t^{0.5}$ dependence could be obtained if a and b are infinite which follows the relationship between failure power and pulse duration by Wunsch and Bell.

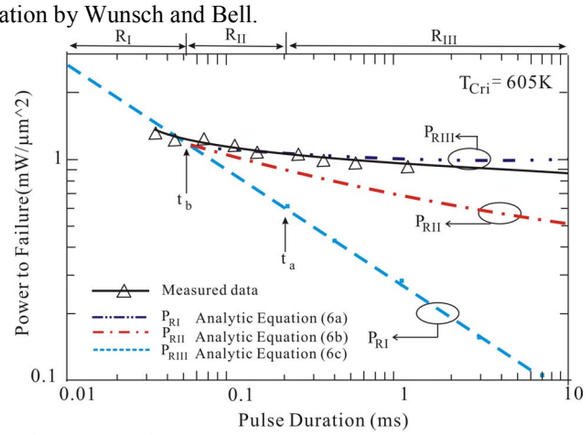
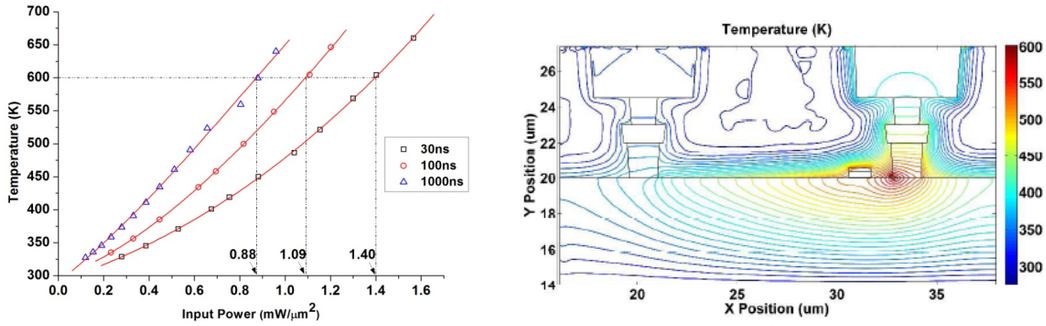


Fig.3. LDMOS FET power to failure data fitting by measurements, simulated and analytic calculations results are also shown.

5. SIMULATION RESULTS AND VERIFICATIONS

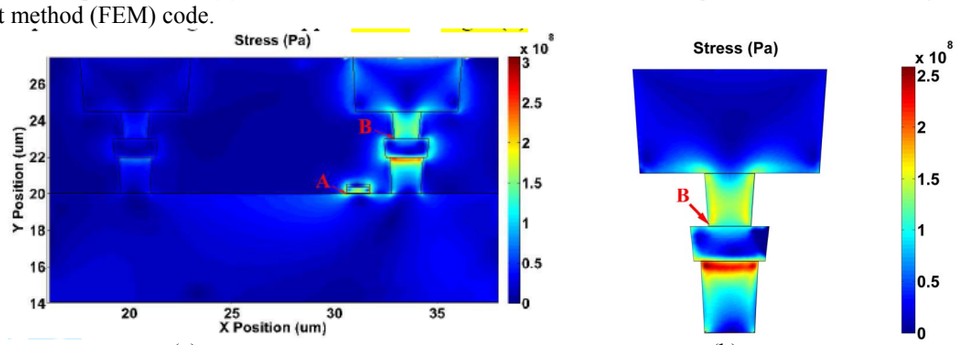
To characterize the maximum temperature of the LDMOS FET, we use our developed time-domain Finite Element Method (FEM) algorithm for simulating active device breakdown. This numerical methodology can simulate the structure of the LDMOS FET. Mesh information, carriers doping distribution, model equations and iterative approach are essential for applying. We also use the preconditioned conjugated gradient technique combined with the element-by element approximate factorization method in order to enhance the computational efficiency, which can reduce error accumulation and provide a fast convergence. Fig.4(a) shows the steady-state simulated maximum temperature of the LDMOS FET verses input EMP signal power level under different pulse width. It is evident that the input power value is higher for shorter pulse width than for longer pulse width. Fig.4(b)shows its maximum transient thermal distribution under a 1-µs pulse, injected into the drain, with a measured breakdown power of 0.9 mW/µm^2. The bottom boundary of the silicon region is set to be a heat sink at 300 K. The hot spot lies between the drain and the gate. Joule heat is mainly generated in the silicon region between the drain and the gate, where it accumulates rapidly.

Fig. 5(a) shows the maximum transient stress profile when the maximum temperature is reached, under a 1-µs pulse width. The maximum stress of the structure is located at point A, on the left edge of the gate oxide having a thickness of 10 nm. The maximum stress value at point A is σ_A = 310.5 MPa. An enlarged view of the drain electrode is shown in Fig. 5(b). Compared with copper, the heat conductivity of tungsten is smaller, and causes thermal incubation at the boundary of the two metals, where the maximum stress of the drain via is approximately 258.6 MPa.



(a) (b)

Fig.4. (a)Steady-state simulated maximum temperature of the LDMOS FET verses input EMP signal power level under different pulse width, (b) the maximum thermal distribution of the integral model simulated by our finite element method (FEM) code.



(a) (b)

Fig. 5. (a) Stress distribution of the integral model by finite element method (FEM) code, (b) magnified view of the stress on the drain electrode by FEM code.

6. Conclusion

In this paper, we have presented detailed experimental results for studying of breakdown of the GaAs MESFET and LDMOS FET under EMP. The measurement system is setup. The electro-thermal-stress breakdown of the LDMOS FET and GaAs MESFET is demonstrated by increasing the specified input pulse power. The threshold power to failure values are recorded under different pulse width. A 2-D analytic model has been used in order to extract the thermal breakdown temperature based on the experimental power to failure data. By using our developed algorithm, we are able to characterize the temperature and stress distribution and the transient performance of the semiconductors.

7. References

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8. Acknowledgments

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