Built-In-Self-Test (BIST) Probing for Wireless Non-Contact Measurement and Characterization of Integrated Circuits and Systems

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Abstract

This paper discusses concept and feasibility of wireless BIST probing for non-contact measurement and characterization. Inter-Chip noise interferences as function of wireless coupling-path attributes (*wireless separation distance between emitter and receiver chips, injected power levels, Charge-Pump-Current*) are characterized. Study of BIST for reconfigurability of on-chip functions is investigated based on design of programmable automatic oscillation amplitude control of PLL reference oscillators. Impacts of BIST circuits on system performances are evaluated based on simulation analysis and experimental verifications.

1.Introduction

Reconfigurability represents key features for multi-mode and multi-standard functionality and Cognitive Radio applications. As an ultimate reconfigurable system, Cognitive Radio [1] is the achievement of Software-Defined Radio (SDR) platform evolution: a fully reconfigurable radio that changes its communication modules depending on network and/or user awareness and demands. Among main objectives of SDR are possibilities to produce communication devices which can adapt their hardware functionality in function of the wireless network systems e.g., GSM, UMTS, wireless WAN/LAN standards such as IEEE 802.11a/b/g. However, reconfigurability can impact global performances and reduce margins in system specifications over temperature, power supply and process variations. Although significant efforts have been directed towards developing reconfigurable solutions, in published investigations very limited attention has been devoted to impact of reconfigurability on system performances. The capability of controlling integrated individual circuit blocks for evaluating their input and output signals is necessary to validate their performances and lower test-verification cost as well. Built-in-Self-Test (BIST) solutions designed as sensors to incorporate within circuit blocks to detect, at identified internal nodes, their input/out signals is seen very promising. The input/output signals sensored by BIST circuits can be further processed and used to validate design performances against reference system specifications. To address test cost issue for productivity enhancement, important research efforts are being directed to developing cheaper and effective BIST solutions [2-3]. With existing BIST solutions main challenges are proper interfacing between RF/Microwave and digital domains for efficient implementation including signal processing control.

This paper discusses BIST probing for wireless non-contact measurement and characterization of integrated circuits and systems. Classical BIST techniques were essentially implemented in off-chip configurations, and recent research efforts have considered moving the tests and detections to on-chip systems. Having BIST modules [2-3] within the chip renders possible sensoring internal nodes of integrated functions for direct performance detection, control and reconfigurability. Combining BIST techniques for assessment of circuit performances based on specified metrics (*gain, IP3, phase-noise, etc…*) with digitally-controlled reconfigurability opens new possibilities for optimization of system functionality. In this work, proposed feasibility studies of BIST for reconfigurability of on-chip functions cover design of programmable oscillation amplitude control of integrated PLL reference oscillators [5]. Impacts of BIST circuits on system performances are evaluated based on careful correlation analysis between simulation and measurement. Perspectives for wireless BIST achieving non-contact monitoring and measurement based on the use of on-chip antenna for mmWave, Microwave and THz frequencies are seen very promising [7].

2. Description of Wireless Chip-to-Chip Interference and BIST PLL Regulation

A. Chip-to-Chip Wireless Interferences

Three entities are distinguished: the *Emitter* (or aggressor), the *Receiver* (or victim) and the *coupling-path*. A real-world wireless car access transceiver chip is used as applicative carrier for investigating inter and intra-Chip interferences and couplings. For the interference and coupling analysis complete PLL circuits (*highlighted in Fig.1*) is identified as

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critical sensitive block for the role of aggressor and victim as well. The chip carrier with microphotograph shown in Fig.1(c) represents a low power transceiver System on Chip (SoC) integrated circuit, working around 868MHz, dedicated to automotive application for secure vehicle immobilization and car access. The automotive chip is designed with NXP's QUBIC4(plus) BiCMOS technology based on 5 levels of stack metallization in the back-end. The silicon die has a dimension of 2.340×1.880mm², a die-pad of 3.80× 3.80mm² and the whole solution is integrated into a HVQFN32 package. A functional diagram of the automotive chip circuit is shown in Fig.2(a).

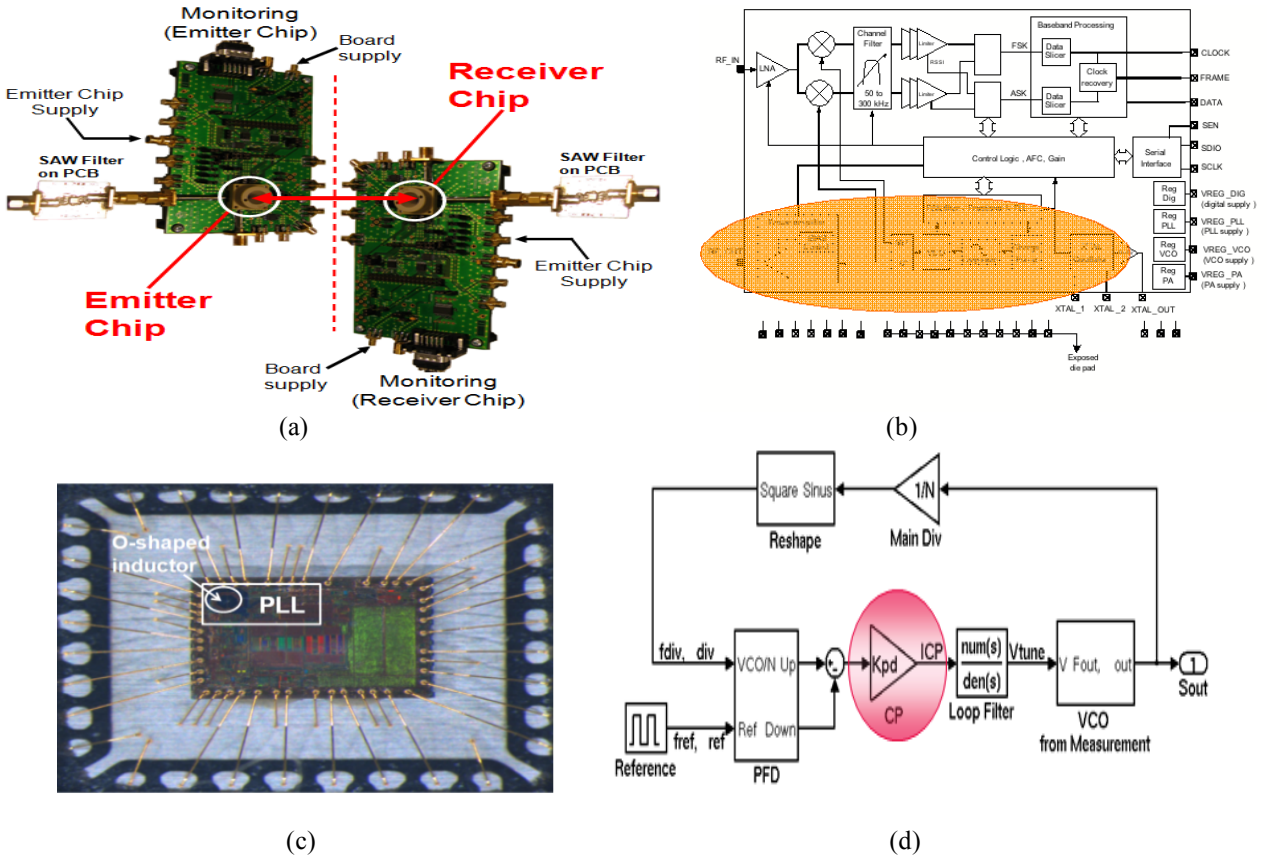


Figure 1: Measurement setup of chip-to-chip wireless interference (a), functional block diagram of wireless car access transceiver (b) with highlighted TX part, microphotograph of chip design (c), dynamic behavioral model of PLL system (d).

The analysis of inter-Chip couplings and interferences is carried out based on the following effects in reference to the wireless chip-to-chip communication setup in Fig.1(a), using :

- *Influence of Chip aggressor (transmitter) power-level on Chip victim (receiver) frequency pulling for different chip-to-chip distance*
- *Impact of Chip aggressor (transmitter) power-level on Chip victim (receiver) frequency pulling for different chip-to-chip distance.*
- *Impact of Chip aggressor (transmitter) PLL Charge-Pump-Current(ICP) level on Chip victim (receiver) frequency pulling.*

Two identical transceivers (using the low power automotive chip in Fig.1(c)) in transmit mode reported (soldered) on their test PCB are placed face-to-face so that the VCO inductances are lined up. So the surface of the chip for aggressor and the surface of the chip for victim are opposed. The chip aggressor working frequency f is fixed to f_0=868MHz and the working frequency of the receiver (victim) chip is set at a frequency slightly different from f_0.

The characterization results of the inter-chip coupling analysis are based on the measurement of power spectrum for evaluation of pulling and pushing effects both at transmitter and receiver sides. Because of mechanical constraints in link with the PCB fixture for the alignment of the transmitter and receiver chips minimum separation distance between the chips is set to 0.8cm. Fig.2 shows measured output power spectrum variation of the chip victim as function of the distance between the chips (*measurement results for two separation distance, namely 0.8cm and 2 cm are reported*). Higher spurs levels are observed for lower separation distance with noise excess exceeding 10dBm differential power when separation distance is reduced from 2cm to 0.8cm.

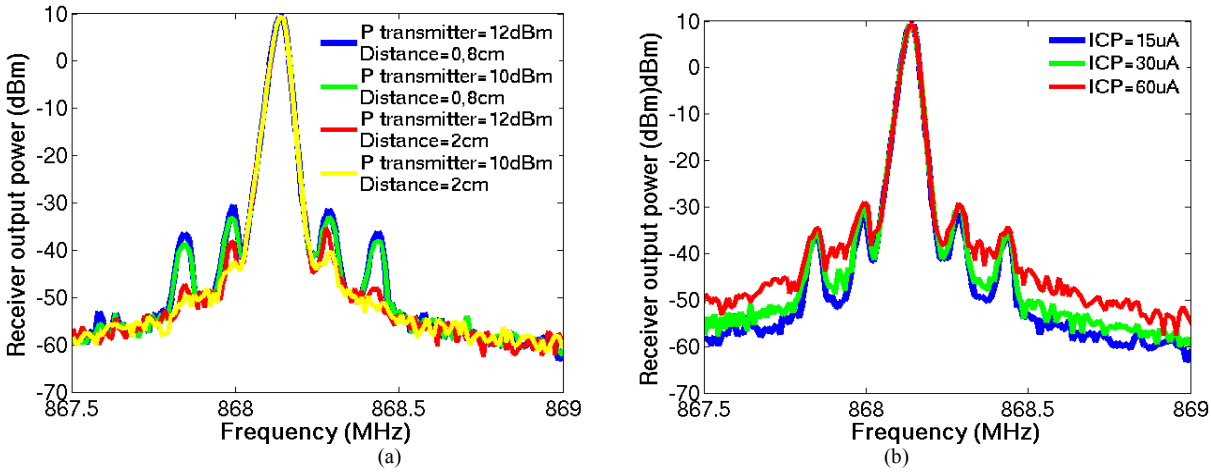


Figure 2: Measured output power spectrum variation of the chip victim as function of output power-level of the chip agressor (P transmitter) and the distance between the chips (a).Measured output power spectrum variation of the chip victim as function of its charge pump current (ICP) value(b).

Inter-Chips interaction can also lead to frequencies pulling as underlined in [4] and [8] that are due to intra-Chip couplings interactions. Higher amplitude of the injected signal in the VCO/PLL of the victim, lead to higher spurs amplitude around the fundamental tone. In Fig.2(a), the power level of the aggressor chip is varied from 10dBm to 12dBm. In Fig.2(b) we can see that the charge pump current value of the Chip victim PLL affects the noise level around the fundamental tone to transmit; if the level of the injected signal is low enough, the frequency pulling effects can be hidden by the noise level around the fundamental tone.
In [4] experimental characterization of VCO nonlinear parameter K_{VCO} has showed links between pulling in PLL and appearance of discontinuities in the frequency response of the VCO transfer function *(K_{VCO} as function of tuning voltage)*. The experimental characterization are confirmed by dynamic behavioral modeling using Simulink for the analysis of the complete PLLs loop. So BIST for detecting PLL spectrum signature will give straightforward ways for verifying proper functionality of the synthesis system.

B. BIST System for PLL Regulation

The proposed BIST system for PLL regulation is applied to frequency synthesis of microwave downconverter for satellite TV receiver application. Its function is to convert the antenna signal in range at 10.7-12.75GHz down to a satellite TV IF band in range 950-2150 MHz. Fig.3(a) shows the block diagram of PLL circuit. The Local Oscillator global phase noise when the PLL is locked should be: -86 dBc/Hz at 10kHz offset, -89 dBc/Hz at 100kHz offset, -107 dBc/Hz at 1MHz offset and -130 dBc/Hz at ≥10 MHz offset from f_{LO}. The PLL uses on-chip crystal oscillator working at different frequencies supporting various types of low cost quartz resonators. The BIST regulation system shown in Fig.3 is introduced to allow for dynamic control of reference oscillation amplitude and frequency to ensure stable phase-noise performances over temperature and process variations. The amplitude level regulation mechanism uses integrated MOS RMS detectors and a comparator with a reference power level. The reference oscillation power-level is programmable using digital bits accessible trough I²C bus for test and evaluation purposes.

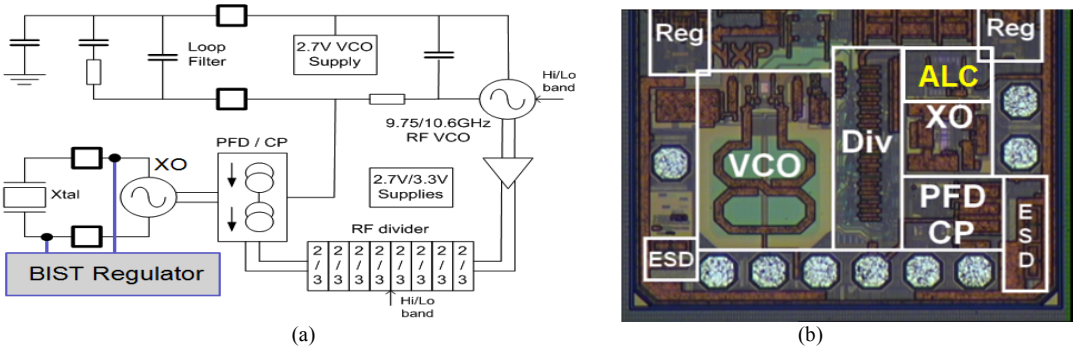
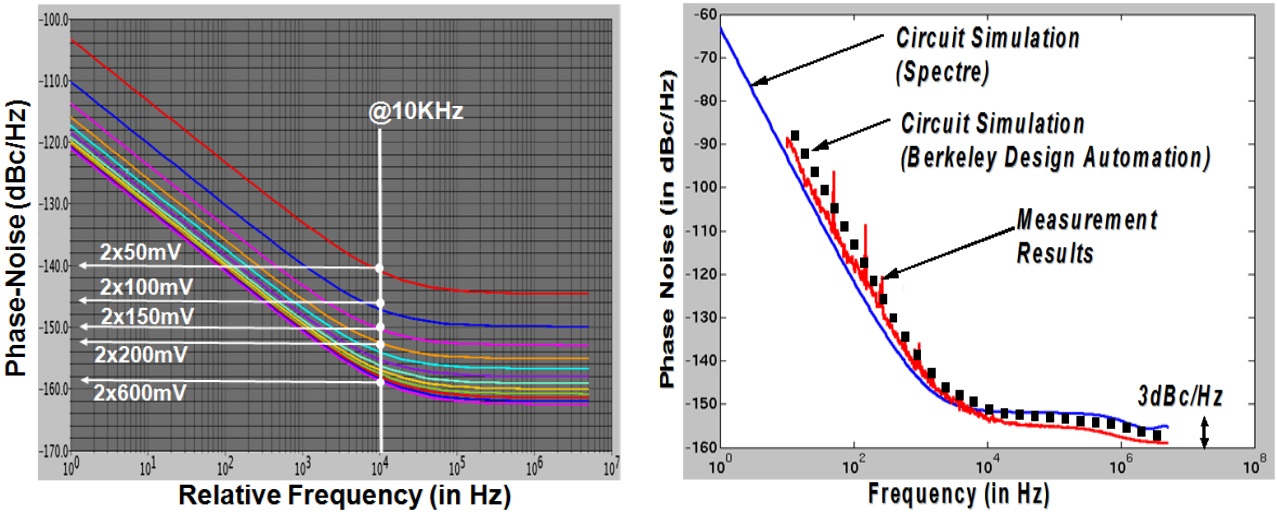


Fig.3 Bloc diagram of designed PLL (a) with integrated BIST(ALC), Microphotograph (b) of PLL circuit block.

3. Main Results, Analysis, Experimental Characterization and Verification

Fig.4(a) illustrates PLL reference oscillator phase-noise as function of automatic amplitude-level control (ALC). The automatic ALC level is set using digital bits. Both MOS and CML ALC BIST [6] control have been designed fabricated and compared. In Fig.4(b), because of saturation effects, nonlinear dependence of crystal resonator quality factor on power drive-level, etc... higher oscillation power-level does not necessarily lead to better phase-noise performances [5-6]. Simulation results of phase-noise are in excellent agreement with measurement.



(a) (b)

Fig.4 Effects of automatic ALC regulation level on oscillator phase-noise (a), correlation between simulation and measurement (b).

Observed differences with Spectre analysis result from phase-noise convergence against number of harmonic sidebands. BDA analysis assumes infinite number of harmonic sidebands. The experimental results demonstrate extremely low phase noise performances below –162dBc/Hz at 50MHz.

4. Conclusion

This paper has proposed feasibility study of BIST probing for wireless non-contact measurement and characterization of integrated circuits and systems. Application of BIST regulation, monitoring and control to design of programmable automatic oscillation amplitude control of PLL reference oscillator has been discussed. In the application of BIST regulation to PLL reference oscillator control, although introduction of BIST circuit induces very limited additional consumption (*less than 2%*), it can increase noise in the PLL regulation loop (*with excess up to 3dBc/Hz*) especially for large dynamic amplitude control). At inter-Chip level, impact of wireless coupling-path attributes such as chip-to-chip distance, and emitter chip power-level and Charge-Pump-Current on PLL pulling has been experimentally evaluated. Use of BIST for detecting PLL spectrum signature is proposed for verifying proper functionality of the synthesis system.

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