Phase Redress for the Bend on Differential Microstrip Lines

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Abstract

The bend is often encountered in routing the differential microstrip lines on PCB layers for high-speed transmission. In addition to generating unwanted electromagnetic wave in air, a bend of differential transmission line also causes random ultra phase difference other than 180 degree for the original odd mode. In this paper, the effect caused by the bend of differential microstip line is demonstrated and analyzed. Importantly, a technique for redressing the ultra phase difference is proposed. Both of simulation and measurement results are presented in this work.

1. Introduction

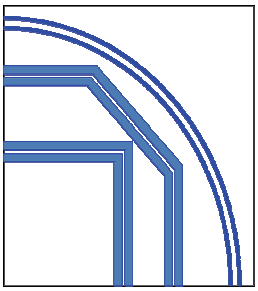

Fig. 1 Illustration of the bends of differential transmission lines

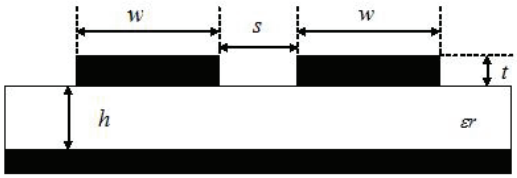

Fig. 2 Cross section of a pair of differential lines on a PCB

Because of the need of low voltage yet high speed transmission [1] for digital signals running in the up-to-date communication and consumer components or products, for example, HDMI connectors [2], LCD panels [3] and mobile phones, the structure of differential transmission line [4] has been widely adopted for the signal propagation on hardware. It can be realized either by the 3-dimentional mechanical structure in a connector or on the planar layer of PCB. In terms of physical form, a pair of differential transmission line is composite of two individual lines as shown in Fig. 1. If it is made within PCB layers, it is of the structure of microstrip lines [5] as shown in Fig. 2. Two conducting traces of width "w" are placed in parallel with a certain distance "s", and are above a ground plane. On the other hand, electrically, being in an odd mode, there are two signals with 180 degree phase difference running along this structure. The common-mode noise will be perfectly rejected if such a structure is kept along the propagation path.

However, when the traces are routed and laid on the PCB layers, bends are necessary when the direction of path is changed as shown in Fig. 1. Consequently, in addition to generating electromagnetic unwanted wave in air, such a kind of discontinuity of transmission line will cause further random phase difference other than the exact 180 degree, then the perfect odd mode structure is destructed. Complex bends are often associated inside high-speed connectors [2] because of the space limitation and mechanical requirements.

In this paper, the effect caused by the bend of differential microstip line is demonstrated and analyzed. Importantly, a technique for redressing the ultra phase difference are proposed. Both of simulation and measurement results are presented in this work.

2. Problem Statement

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As a demonstration, Fig. 3 shows a bend of differential microstrip lines, which is modeled by the electromagnetic simulation tool – CST [6]. By applying two sine waves of 1GHz in phase simultaneously on the input ports of those two microstrip lines, the outer (longer) line of this pair exhibits a phase delay of 9.6556° as shown in Fig. 4. Obviously, such a phase delay will worsen the exact 180° phase relationship of differential line if the odd mode is propagating. When being so, the main feature of common-mode noise rejection is not guaranteed any more.

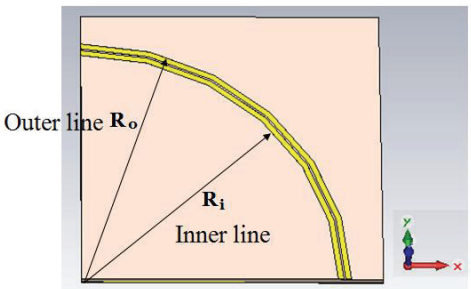

Fig. 3 A simulated model of a bend of the differential microstrip lines

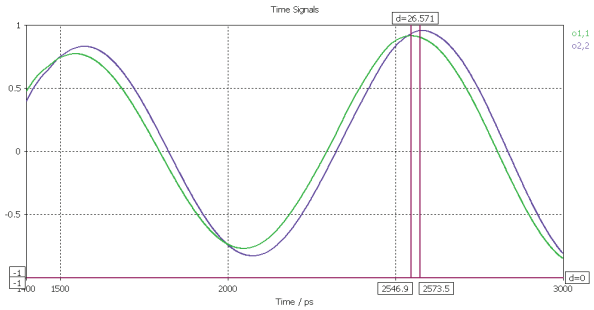

Fig. 4 Phase difference caused by a bend

In the work [7], the analysis of bend of differential microstrip lines mentioned above had been carried out, and a technique by laying one parallel parasitical line on either side of that transmission structure had been proposed and proved to be capable of successfully adjusting this phase difference in between the original two lines. Hence, by the help of simulation tool, a phase redress procedure is established for further engineering aim.

3. A Proposed Method for Phase Redress

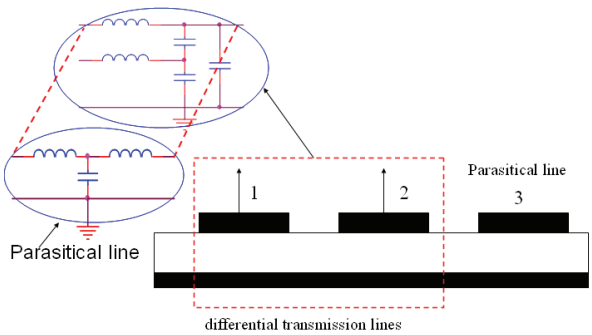

Fig. 5 Circuit effect when a parasitical line is added

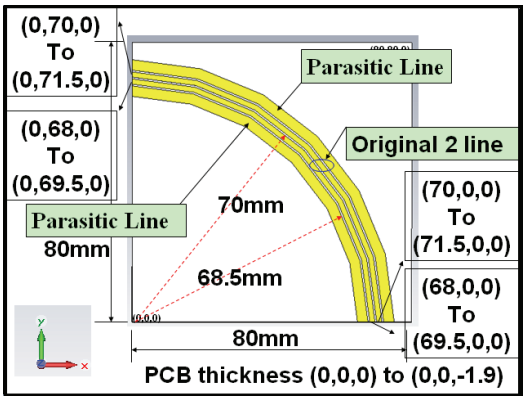

Fig. 6 Detail dimension of a test bed

In terms of circuit theory, when laying out another parasitical trace along the original differential microstrip lines, extra coupling electrical and magnetic reactive components are created, see Fig. 5. Then, the one of differential microstrip lines which is by the side of parasitical trace will be influenced either with attenuation or phase delay. By such an idea, around the bend, the parasitical trace can be functioning to do phase redress for the original pair of coupled lines.

For demonstrating this technique, a test bed either being a simulation model for computer EM package or a realized PCB, has been designed and fabricated. Its detail dimension is shown in the Fig. 6, in which, the parasitical traces are planed for further evaluation.

Two input signal (Sine step wave Freq.)	1GHz	2GHz	3GHz
Orginial Bend of differential lines	Reference phase = 0˚ Phase delay 9.648 ˚ (lag 26.8pS)	Reference phase = 0˚ Phase delay 23.062˚ (lag 32.03pS)	Reference phase = 0˚ Phase delay 41.29˚ (lag 38.2pS)
Parasitic W=1.5mm line at inner side	△phase = -2.051˚ Phase delay 7.597 ˚ (21.103pS)	△phase = -2.87˚ Phase delay 20.232˚ (27.81pS)	△phase = -3.452˚ Phase delay 37.838˚ (35pS)
Parasitic W=3.0mm line at inner side	△phase = -5.457˚ Phase delay 4.191 ˚ (11.641pS)	△phase = -4.572˚ Phase delay18.49 ˚ (25.68pS)	△phase = -4.436˚ Phase delay 36.854˚ (34.09pS)
Parasitic W=4.5mm line at inner side	△phase = -7.406˚ Phase delay 2.242˚ (6.2291pS)	△phase = -12.644˚ Phase delay 10.418˚ (14.47pS)	△phase = -16.425˚ Phase delay 24.865˚ (23pS)
Parasitic W=9.0mm line at inner side	△phase = -18.796˚ Phase leading 9.148˚(25.41pS)	△phase = -31.032˚ Phase leading 7.97˚(11.07pS)	△phase = -43.344˚ Phase leading 2.054˚(1.9pS)
Parasitic W=1.5mm line at outer side	△phase = 5.568˚ Phase delay 15.216˚ (42.268pS)	△phase = 14.543˚ Phase delay 37.605˚ (52.23pS)	△phase = 26.18˚ Phase delay 72.432˚ (67.47 pS)
Parasitic W=3.0mm line at outer side	△phase = 8.933˚ Phase delay 18.581˚ (51.613pS)	△phase = 23.112˚ Phase delay 46.17˚ (64.13pS)	△phase = 46.56˚ Phase delay 87.85˚ (81.27 pS)

Table 1 Simulation of phase delay

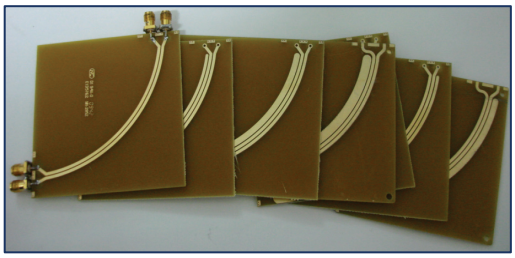

Fig. 7 Realization of test beds

By the help of simulation tool of CST, Table 1 shows the results of phase delay analysis. Fig. 7 shows the realization of test beds for analysis. For an original bend of two parallel lines, as mentioned above, the outer one will be resulted in a phase delay, yet being dependent on operating frequency. It is 26.8ps, 32.03ps and 38.2ps increasingly, as for 1GHz, 2GHz and 3GHz, respectively. By this Table, it is found that, the delay is reduced when the width of an inner parasitic trace is increased for a certain operating frequency. But this conclusion is opposite if the trace is put as an outer one. Therefore, by such an observation, one can adjust the phase difference to be that exactly wanted, for example, zero degree for even mode or 180 degree for odd mode on the parallel microstrip lines under investigation.

Table 2 shows the comparison between the results of CST simulation and the ones of measurement. The case of 3GHz operating frequency is specially explained. Generally, they are easily coincided with each other when the parasitic trace is laid on the inner side. This is an important comment for engineers when they are designing the bends. With a trace of 9mm width, the parallel lines can be adjusted to be in phase after running a bend. As a result, when the pair is applied with signals in odd mode, exact 180 degree can be ensured when being measured at the output of the bend. It should be noted that, the parasitic trace is floated without being grounded.

	CST Simulation	Measurement
Two input signals (Sine step wave Freq.)	3GHz	3GHz
Original Bend of differential lines	Reference phase = 0° Phase delay 41.29° (38.2ps)	Reference phase = 0° Phase delay 40.864° (40ps)
Parasitic W=1.5mm line at inner side	△phase = -3.452° Phase delay 37.838° (35ps)	△phase = -3.024° Phase delay 37.84° (35ps)

Parasitic W=3.0mm line at inner side	△phase = -4.436° Phase delay 36.854 (34.09ps)	△phase = -8.432° Phase delay 32.432° (30ps)
Parasitic W=4.5mm line at inner side	△phase = -16.425° Phase delay 24.865° (23ps)	△phase = -17.293° Phase delay 25.95° (24 ps)
Parasitic W=9.0mm line at inner side	△phase = -43.344° Phase leading 2.054° (1.9ps)	△phase = 0° Phase leading 0° (0ps)
Parasitic W=1.5mm line at outer side	△phase = 26.18° Phase delay 72.432° (67.47 ps)	△phase = 8.65° Phase delay 51.892° (48ps)
Parasitic W=3.0mm line at outer side	△phase = 46.56° Phase delay 87.85° (81.27 ps)	△phase = 17.3° Phase delay 60.54° (56 ps)

Table 2 Comparison between simulation and measurement of phase delay

4. Comments and Conclusion

In this work, an innovative method for phase redress for a bend of differential microstrip lines is presented. Simply adding parallel parasitic trace along the transmission line, the delayed phase can be adjusted to be in-phase. Namely, the necessary 180 degree phase difference can be ensured when the differential signals run and pass the bend. Both results of simulation and measurement are reported.

5. References

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