Ultra-dense Monolithic Integration of Optical and Electrical Functions on Silicon for Optical Interconnects

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Abstract: CMOS Integrated Nanophotonics which allows dense monolithic integration of optical and electrical functions on the same chip can enable future Exaflops supercomputers by connecting racks, modules, and chips together with ultra-low power massively parallel optical interconnects.

High-performance computing (HPC) systems capable of delivering Exaflops performance are envisioned to become a reality by the end of this decade. In order to provide the enormous communication bandwidth that is necessary, hundreds of millions of optical interconnects will have to be deployed to connect together racks, modules and chips. To achieve such massive level of parallelism for HPC systems, monolithic integration of deeply scaled silicon optical circuits into the front-end of standard CMOS process have been demonstrated as a promising technology [1-3].

The monolithic integration of electronic and nanophotonic components was performed at the IBM using 200 mm SOI wafers (SOITEC) having a 220 nm silicon device layer on top of a 2 μm BOX [1-4]. Several processing modules have been added to a standard CMOS processing flow at the front-end of the line. These modules require a minimal number of additional unique masks and processing steps, while sharing most mask levels and processing steps with the rest of CMOS. For example passive waveguides and electro-optical and thermo-optical modulators share the same silicon device layer with CMOS PFETS and NFETS. The Ge waveguide photodetectors were fabricated by utilizing a rapid melt growth (RMG) technique wherein the Ge was melted and crystallized during the source-drain anneal step [5-6]. As opposed to traditional approaches where Ge is typically grown by CVD after the source-drain anneal step, the RMG approach enables the sharing of many CMOS steps and mask levels, thus minimizing cost, while yielding a very thin defect-free Ge layer.

After completion of the monolithic integration including the metallization levels, the waveguides (200 nm x 500 nm cross-section) exhibit propagation loss below 3dB/cm and bending losses less than 0.02dB per 90^{o}-bend with 6 μm radius. Also, a cascaded Mach-Zehnder (CMZ) 8-channel WDM filter provided 8 flat-top 2 nm-wide pass-bands with in-band ripple less than 1 dB and cross-talk less than -10 dB [7]. Furthermore, reverse-biased modulators were demonstrated to have flat RF response with a 3 dB cutoff exceeding 20GHz [8], while the Germanium photodetectors showed 3dB cutoff beyond 40 GHz at 1.5-2.0 V bias with some devices producing up to 10 dB avalanche gain at the same low bias conditions [9].

The CMOS ring oscillator (RO) testsite is taken from a standard IBM digital library and consists of a 65-stage ring oscillator, 10-stage ripple counter, and 4-stage divider (Fig. 1a)). After integration of all nanophotonics processing modules the RO exhibits 12 ps delay per stage at saturation, under a 1.5 V bias. This performance is on-target for 130 nm bulk technology.

The receiver amplifier (Fig. 1b)) consists of a DC-coupled common-gate transimpedance amplifier (TIA) occupying 170 μm x 40 μm, followed by a cascade of seven current-mode logic (CML) buffer limiting amplifier (LA) stages, followed by a single-ended open-drain output driver. The total area occupied by the multi-stage LA and output driver is 160 μm x 50 μm. The total circuit area is dominated by decoupling capacitors used to minimize the supply voltage noise. After incorporation of all nanophotonic processing modules, the receiver amplifier exhibits an open eye diagram at 5 Gbps with total power dissipation of about 28 mW (5.6 pJ/bit).

The modulator driver (Mod DRV) circuitry (Fig. 1c)) consists of the input pre-driver (105 μm x 175 μm) made of a 6-stage differential CML amplifier, and an output stage (105 μm x 70 μm) consisting of a cascoded differential driver with a dedicated power supply. The total circuit area is similarly dominated by the decoupling capacitors. High-speed operation of the output stage is enabled by a differential pair of low-threshold thin oxide NFETs. High-voltage, high-output swing capability of the output stage is enabled by a pair of long-channel thick oxide devices in a cascode configuration, protecting the thin oxide devices from the output voltages. After incorporation of all the nanophotonic processing modules, the transmitter amplifier exhibits an open eye diagram at 5 Gbps with total power dissipation of about 36 mW (7.2 pJ/bit).

Figure 2 contains die photographs of a 6-channel transmitter (Fig. 2a)) and 6-channel receiver (Fig. 3b)). The chip footprint of the transmitter in Fig. 3a) (counted as shown by the dotted outlines in Fig. 1b)) is 3700 μm x 350 μm. The 0.21 mm2 area per channel is limited by the pad frame and decoupling capacitors. The area of the 6-channel receiver

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(Fig. 2b) counted the same way is 3700 µm x 500 µm, which totals to an area of 0.31 mm2 per channel. Correspondingly, the area per single transceiver channel can be estimated as 0.52 mm^2, which is approximately 10 times smaller than previous demonstrations [10].

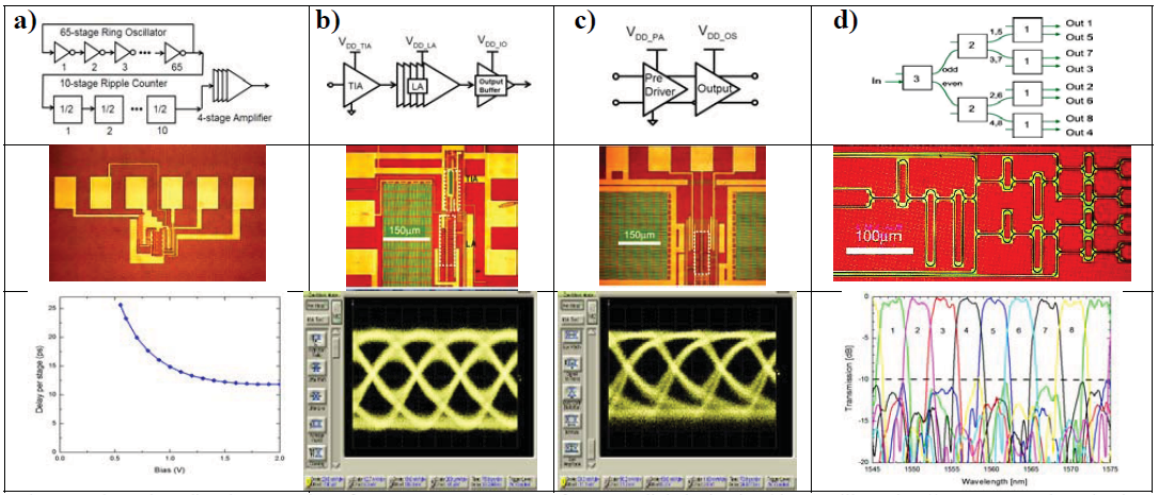

Fig. 1. Schematics, die photos, and performance measurements of CMOS digital circuits (ring oscillator in a)), CMOS analog circuits (transimpedance amplifier in b), modulator driver amplifier in c)), and nanophotonic circuits (cascaded Mach-Zehnder WDM in d)), taken after completion of the full integrated process flow.

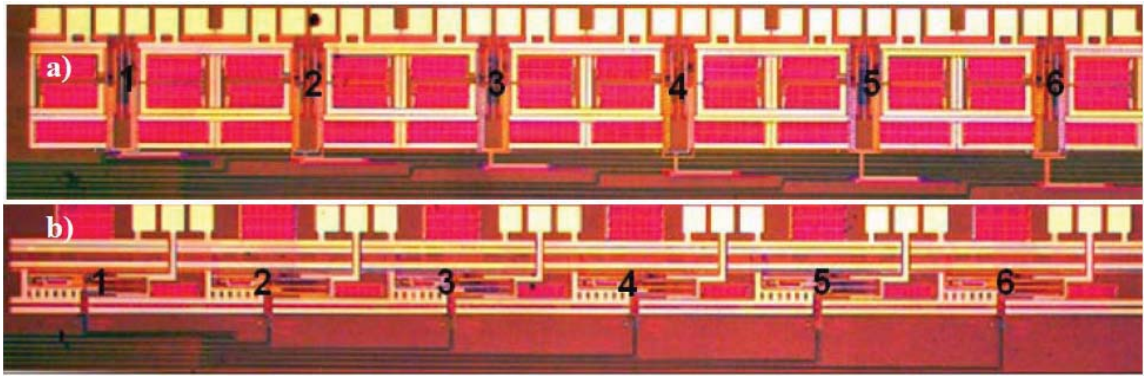

Fig. 2. Micrographs of an integrated silicon nanophotonic a) 6-channel transmitter and b) 6-channel receiver.

To conclude, a proof-of-principle demonstration of dense monolithic integration of silicon nanophotonic components with analog and digital CMOS circuitry has been described. The integration density offered by the technology is at least 10 times higher than previous reports. The technology offers a scalable solution for massively parallel Terabit/sec-class optical transceivers, with 50 channels supporting serial lines rates of 20 Gbps each, occupying only 4 mm x 4 mm on a single CMOS die.

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