Generalized Parameter Extraction Model for High-Speed Interconnects with Arbitrary Boundary Conditions

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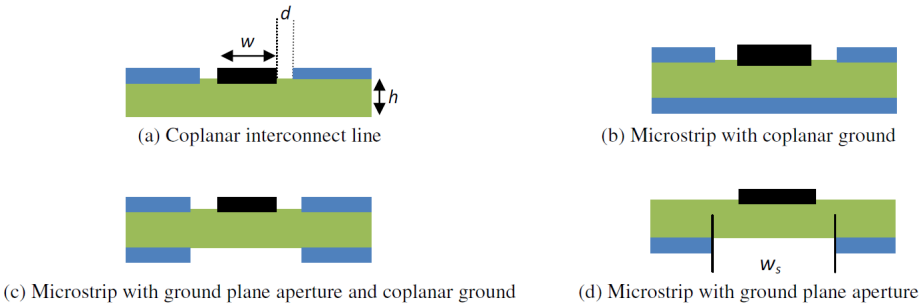
Abstract

An accurate and general interconnect model for planar transmission line interconnects with arbitrary boundary conditions is presented. Based on the unified approach, we develop new *SPICE*-compatible parameter extraction algorithm that can be used in performance driven computer-aided-design applications. A range of multilayered interconnects with arbitrary boundaries are analyzed. Different ground configurations with respect to the interconnect line are considered for verification of the model. Results are obtained for admittance, line parameters and delay giving physical insights on the effect of boundary conditions. Compared with industry standard field-solvers, our proposed model demonstrates more than 10X speedup within 2% accuracy.

Keywords- High-speed interconnects, parasitic extraction, boundary conditions and computer-aided-design.

1. Introduction

In conjunction with the requirement of miniaturization of devices and interconnects, design trends lead to a situation, where, designers do not have the luxury of indulging in repeated full-wave simulation of the design, specifically for high-speed layout design. Thus, it is now becoming imperative to use circuit models [1, 2] at the beginning followed by final verification, done using full-wave simulators; the emphasis being on reduced time-frame while maintaining reasonable accuracy. Miniaturization efforts have resulted in significantly increased component density on a mixed-signal board. Also, conventional methods for printed circuit board (PCB) trace design with neat ground layers are no longer feasible in most of the design efforts [3, 4]. Thus the performance of such interconnects is critically dependent on the proximity of ground trace (or absence of such) in both multilayer and co-planar configurations. There is need for routing of PCB traces, where PCB trace in one layer sees small windows of aperture in the ground plane in the adjacent layer [5]. Similarly co-planar ground proximity may not run uniformly throughout the entire run of the interconnect line. Also, the typical problem of signal integrity issues in dense layout continues to pose problems [6-7]. Therefore, we need compact models that computes quickly and accurately the various line parameters for an arbitrary placement of ground, thus reducing the design cycle time through intuitive, yet rational, routing scheme of the interconnect and ground trace. Fig. 1 illustrates some of the modified interconnect structures resulting from arbitrary placement of ground. These structures exhibit alteration in the position of ground plane compared to a standard microstrip/stripline. This can complicate analysis as well as parasitic extraction. In this paper, we propose a novel admittance computation and parameter extraction algorithm that generates SPICE-compatible distributed circuit parameters, based on the unified approach [8]. The model is validated by full-wave simulations using HFSS. The results presented here highlight variations in delay, impedance etc. due to such irregular and arbitrary placement of ground.



(a) Coplanar interconnect line
(b) Microstrip with coplanar ground
(c) Microstrip with ground plane aperture and coplanar ground
(d) Microstrip with ground plane aperture

Fig 1 Different interconnect layouts with possible alterations in ground placement
substrate; ground; interconnect

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2. Admittance Computation and Parameter Extraction Algorithm

Advanced modeling approaches and simulation techniques are used to achieve first-pass design success in analyzing the electrical performance of interconnect lines [1-4]. Our proposed model uses the unified approach, which is simple and generalized due to the ease of computing Green's function using the transverse transmission line technique and gives fairly accurate results without much computational effort [8, 9]. For comprehensive review of the unified approach, interested readers may refer to [4, 8, and 9]. Based on the boundary conditions (electric and/or magnetic), the Green's function is computed from the admittance at the charge plane. The equivalent circuit parameters can now be extracted using the variational formula for line capacitance (C) per unit length given by (1) and inductance and resistance formulation given by (2) and (3), respectively. Here, C^a is the line capacitance when the dielectric is replaced by air, and v^a is the velocity of propagation in air. At high frequencies we may use frequency dependent $R_{ac}(f)$ for more accurate resistance extraction [10]. The detailed admittance computation and parameter extraction algorithm is summarized in Table 1. It can be either programmed as post-extraction software or combined into an extraction tool. Based on the proposed algorithm, admittances for Fig. 1 are computed in Table 2.

$$C = \frac{(1+0.25A)^2}{\sum_{n\,odd}\left((L_n + AM_n)^2 P_n / Y\right)}$$

$$where$$

$$L_n = \sin(\beta_n w/2),\ P_n = (2/n\pi)(2/\beta_n w)^2,\ \beta_n = n\pi/c$$

$$M_n = (2/\beta_n w)^3\left[3\left\{(\beta_n w/2)^2 - 2\right\}\cos(\beta_n w/2) + (\beta_n w/2)\left\{(\beta_n w/2)^2 - 6\right\}\sin(\beta_n w/2) + 6\right]$$

$$A = -\frac{\sum_{n\,odd}\left(L_n - 4M_n\right)L_n P_n / Y}{\sum_{n\,odd}\left(L_n - 4M_n\right)M_n P_n / Y} \qquad (1)$$

$$L = \frac{1}{(v^a)^2 C^a} \qquad (2) \qquad R = \frac{1}{\sigma\, t\, w} \qquad (3)$$

Table 1: Admittance computation and parameter extraction algorithm

Input: Given interconnect geometry, including width (w), thickness (t), substrate permittivity (ε_r), etc.
Output: Admittance at the charge plane $y = y_0$ and *SPICE*-compatible *RLC* parameters per unit length

BEGIN

1. Identify the charge plane $y = y_0$, the interface between two layers, at which the interconnect line of thickness 't' is situated between $y = y_0$ and $y = y_0 \pm t$.

2. Determine the boundary conditions, compute Green' function using identities $\sin\frac{n\pi x}{c}$, $\sin\frac{(2n+1)\pi x}{2c}$ and $\cos\frac{n\pi x}{c}$ being orthogonal between $x = 0$ and c.

3. Develop the equivalent transmission line circuit using the equivalencies $Y_{cj} \equiv \varepsilon_j$ and $\gamma_j = n\pi/c$ or $(2n+1)\pi/2c$. Compute the input and load admittances for all dielectric layers above and below the charge plane.

4. Obtain overall admittances for the regions above and below the charge plane as Y_+ and Y_-, respectively. Compute total admittance Y seen at the charge plane as $Y = Y_- + Y_+$.

5. Compute line capacitance 'C' using (1) and 'Y' from step 4.

6. Compute line inductance 'L' using (2) by equating all dielectric constants to 1 and computing C^a.

7. Determine R using (3); compute skin depth 'δ' according to extraction frequency 'f'. Calculate $R_{ac}(f)$.

8. Compute characteristic impedance 'Z' from steps 5 and 6 above.

END

3. Results

In this section, we present comprehensive results to show the efficiency and accuracy of our proposed model. While there are a limited number of results presented here, there is no geometrical limitation for the proposed model as it is versatile and generic. The proposed model gives *RLC* values that are very close to full-wave simulation results (within 2%) and shows over 10X speedup compared to *FDTD* (CST Microwave Studio) or *FEM* (Ansoft HFSS)

methods, as shown in Fig. 2. Parameter extraction time comparison for the interconnects under study is presented in Table 3. The reduction in computation time may be greater for more complex interconnect systems, which makes it suitable in *CAD*-oriented design tools. The introduction of lateral ground tracks introduces electrical wall while *GPA* leads to approximate magnetic wall boundary conditions [4, 8]. We now discuss the effect of modifications in ground plane on the line impedance, delay and signal overshoots are ringing for the above mentioned interconnects. Percentage variation in delay time due to the presence/absence of ground plane is shown in Table 4. The transient response is obtained by combining the extraction program with circuit simulation program, *SPICE*. Fig. 3 compares the characteristic impedance computed for these interconnects with standard microstrip and stripline. The change in the characteristic impedance is due to increased lateral capacitance.

Table 2: Admittance ($Y = Y_- + Y_+$) based on the arbitrary boundary conditions

($\varepsilon_2 = \varepsilon_r$, $b_2 = h$, b_3 = height of region above charge plane, b_1 = height of region below dielectric)

Fig. 1(a)	**Fig. 1(b)**
$Y_{-,n} = \varepsilon_0\varepsilon_2 \left(\dfrac{\coth\left(\beta_n\left(\dfrac{b_1+b_3}{2}\right)\right)\coth(\beta_n b_2)+\varepsilon_2}{\varepsilon_2\coth(\beta_n b_2)+\coth\left(\beta_n\left(\dfrac{b_1+b_3}{2}\right)\right)} \right)$	$Y_{-,n} = \varepsilon_0\varepsilon_1\coth(\beta_n b_1)$
$\beta_n = n\pi / c, c = 2d + w, n = 1,3,5,...$	$\beta_n = n\pi / c, c = 2.d + w, n = 1,3,5,....$
$Y_{+,n} = \varepsilon_0\varepsilon_3 \coth\left(\beta_n\left(\dfrac{b_1+b_3}{2}\right)\right)$	$Y_{+,n} = \varepsilon_0\varepsilon_2\coth(\beta_n b_2)$
$\beta_n = n\pi / c', c' >> w, b_1 = b_3 >> b_2, n = 2,4,6,...$	$\beta_n = n\pi / c', c' >> w, b_2 >> b_1, n = 2,4,6,...$
Fig. 1(c)	**Fig. 1(d)**
$Y_{-,n} = Y_I + Y_{II} + Y_{III}$	$Y_{-,n} = Y_I + Y_{II} + Y_{III}$
where	*where*
$Y_I = Y_{III} = \varepsilon_0\varepsilon_2\coth(\gamma_m b_2)$	$Y_I = Y_{III} = \varepsilon_0\varepsilon_2\coth(\gamma_m b_2)$
$Y_{II} = \varepsilon_0\varepsilon_2\tanh(\alpha_n b_2)$	$Y_{II} = \varepsilon_0\varepsilon_2\tanh(\alpha_n b_2)$
$\alpha_n = \dfrac{n\pi}{W_S}$ *and* $\gamma_m = \dfrac{m\pi}{g}$	$\alpha_n = \dfrac{n\pi}{W_S}$ *and* $\gamma_m = \dfrac{m\pi}{g}$
$n=1,3,5,...,m=2,4,6,...,g=(c-W_s)/2$	$n=1,3,5,...,m=2,4,6,...,g=(c-W_s)/2$
$Y_{+,n} = \varepsilon_0\varepsilon_3\coth(\beta_n b_3)$	$Y_{+,n} = \varepsilon_0\varepsilon_3\coth(\beta_n b_3)$
$\beta_n = \dfrac{n\pi}{c}, c = 2d + w, b_3 >> b_2, n = 2,4,6,...$	$\beta_n = \dfrac{n\pi}{c}, b_3 >> b_2, n = 2,4,6,...$

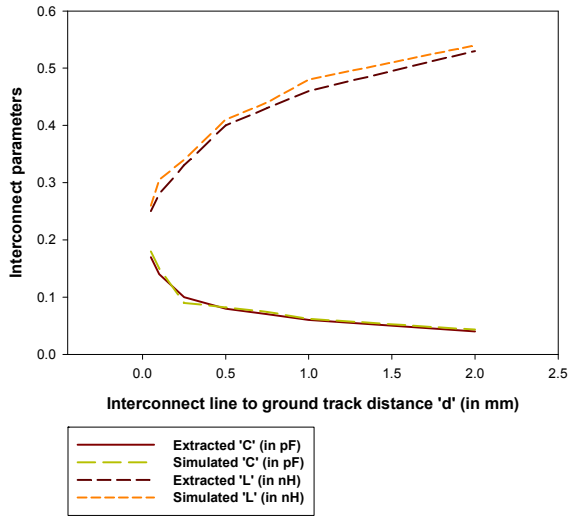
Table 3: Average extraction time using our proposed algorithm

Interconnect structure	Extraction time (in seconds)
Coplanar interconnect line	25
Microstrip with coplanar ground	24
Microstrip with ground plane aperture and coplanar ground	28
Microstrip with GPA	31

Table 4: Percentage variation in delay time due to alteration in ground plane

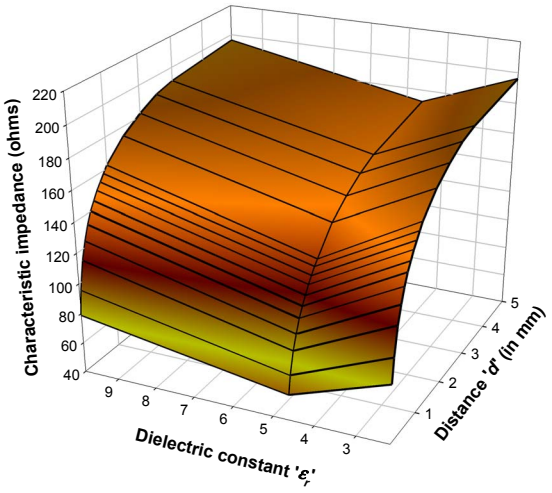
ε_r	h (in mm)	w = 0.5 mm		
		Fig. 1a (d = 0.1)	*Fig. 1b* (d = 0.1)	*Fig. 1c* (Ws = 5)
4.6	0.254	10	75	18
	0.508	18	78	10
	0.79	24	82	5
	1.59	32	81	2

**For, Fig. 1a and 1b, the data represent average % increase in delay time compared to microstrip line and stripline; while for Fig. 1c, it represents average % reduction in delay time compared to microstrip line.



Coplanar interconnect (w = 1 mm, ε_r = 4.6, h = 0.79 mm)

Fig. 2 Comparison by using proposed algorithm and HFSS



Coplanar interconnect (w= 0.2 mm h = 0.508 mm)

Fig. 3 Variation in characteristic impedance

4. Conclusion

This paper presents an accurate and compact interconnect model based on the unified technique for analysis of microstrip-like interconnects with arbitrary boundaries. Experimental results demonstrate the accuracy and efficiency of the model and highlight the effect of ground plane on impedance, delay etc. Readers must note that while a limited number of results are presented here, the proposed model is valid for all practical multilayer interconnects. The proposed algorithm generates *SPICE*-compatible circuit parameters.

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