Status of the Phased-Array Feed Demonstrator at DRAO

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Abstract

The PHased-Array feed Demonstrator (PHAD) project is exploring engineering aspects of this new technology. PHAD comprises 180 active Vivaldi elements operating from 1 to 2 GHz. Each element feeds a low-noise amplifier and a receiver (both commercial integrated circuits), with the outputs digitized and stored. Beamforming is performed off-line using a matrix language, providing great flexibility in diagnostics and algorithm development.

PHAD testing began in a near-field range and has progressed to tests on a 10-m reflector antenna. This presentation will report early results with emphasis on calibration.

PHAD Description

The PHased-Array feed Demonstrator (PHAD) project is exploring engineering challenges of this new technology. It does not have the sensitivity or bandwidth for astronomical observations but instead has been optimized for modularity, experimentation, and ease of fabrication.

PHAD uses Vivaldi elements fabricated on microwave printed-circuit board material. The elements are modular for ease of assembly, as shown in Fig. 1. This element design is well-suited for illuminating reflector antennas since the edge taper for $f/D = 0.45$ (58°) is only $\sim$ 3 dB. An example of a typical radiation pattern is shown in Fig. 2. The array operates between 1 to 2 GHz and has 180 Vivaldi elements in both polarizations. At the highest frequency the element spacing is $\lambda/2$.

Each element feeds a low-noise amplifier and a receiver. Commercially-available integrated circuits (ICs) have been used to expedite development. The noise temperature of the receiver has been measured to be $\sim$100K. The receiver IC uses direct conversion (homodyne) architecture and provides in-phase (I) and quadrature (Q) outputs at baseband with a selectable bandwidth between 4 and 32 MHz. Single-sideband operation is obtained by combining the I and Q channels with a 90° phase shift. This operation is performed in the digital domain where a self-calibration technique corrects for amplitude and phase offsets to ensure

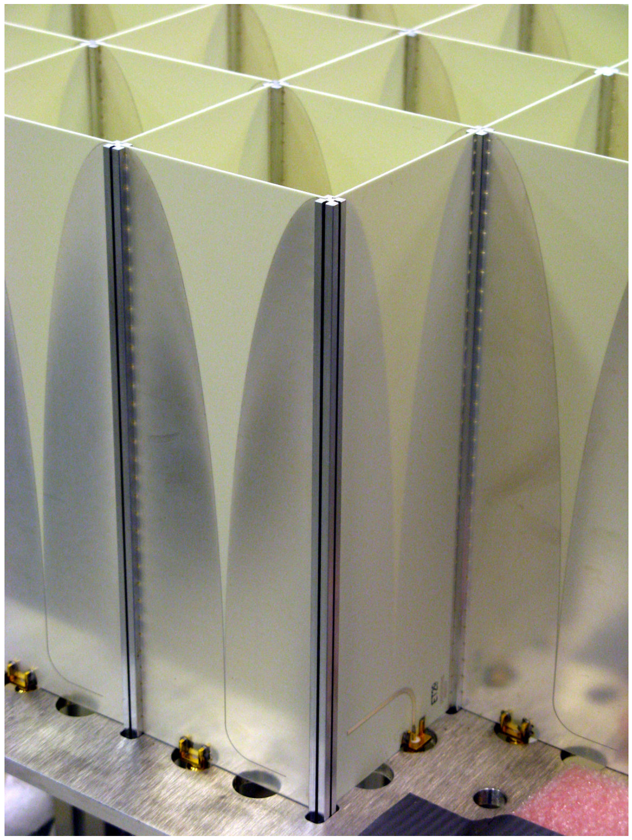

Figure 1: Detail of Vivaldi elements showing modular circuit boards, mounting rails, and backplane. The array is designed to operate over the frequency range of 1 to 2 GHz. The element spacing is 7.6 cm and each element is 20 cm long.

a high level of suppression of the undesired sideband. In addition, working with I and Q channels makes implementation of beamformer phase rotations simple.

From the very beginning, PHAD was designed to store data streams for off-line processing rather than using a real-time hardware beamformer. This enables a level of diagnostics difficult to achieve in a hardware beamformer. Stored data streams are easy to manipulate using common matrix or scripting languages but most importantly, beamformer algorithm development is more flexible in this environment.

The PHAD digital signal processor uses 12 digitizer boards, each of which can sample 16 simultaneous channels at 14-bit resolution at 105 MS/s. Each board has sufficient memory to store several seconds of data. Although the primary mode of operation is data capture and off-line beamforming, each digitizer board has a general-purpose interface bus for interconnectivity and a field-programmable gate array (FPGA) which could be programmed as a real-time beamformer.

The complete PHAD system is shown in Fig. 3. Testing has begun in a spherical near-field range to measure element properties and to qualify electronics and software before progressing to tests on a 10-m reflector antenna.

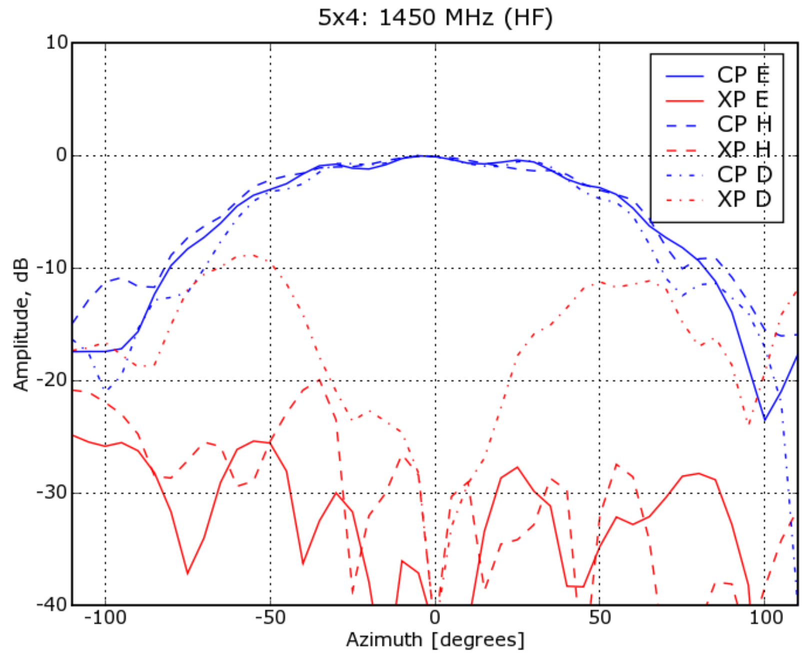

Figure 2: Radiation patterns of an element near the centre of the array at 1.45 GHz. Cuts are made in E-, H-, and D-planes with co- (CP) and cross-polarized (XP) responses. Note that the co-polarized response is similar for all cuts, indicating a circularly-symmetric beam. The cross-polarized response is high in the diagonal cut but we expect to suppress this with appropriate beamformer weights.

Figure 3: Complete PHAD system in the laboratory. To the left is the array with receivers mounted on the rear. The array is 0.76 m $\times$ 0.76 m. The digital signal processor and recorder share the middle rack along with power supplies and signal demultiplexers.