

# A new general purpose high performance HF Radar

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## Abstract

A new HF radar/ionosonde system using digital RF technology is described that matches or exceeds the stringent hardware performance specifications of the 1970 NOAA HF Radar/Dynasonde. A new active antenna preamplifier and front end analog design achieves excellent linearity and low frequency performance from electrically short receiving dipoles. The multi channel receiver uses direct digital RF sampling and down-conversion, providing a wide dynamic range and stable phase matching between channels. The exciter uses flexible digital up-conversion. The radar provides the experimenter with direct network access to raw data for their own processing as well as secure remote control.

## 1. Background

The original NOAA HF Radar (or Ionospheric Sounder) system, now usually known as the Dynasonde or Advanced Ionospheric Sounder, was designed and built by NOAA/SEC in the late 1970's with support from the National Science Foundation. It was designed to be a flexible general purpose tool for making research measurements of the ionosphere by the method of total reflection [1]. The system was an evolution from previous pulse based ionosondes. In particular it embodied the capabilities of the Dynasonde and Kinesonde phase coherent systems [2] that had been developed earlier in the Boulder Laboratories. However by employing later analog and digital technology, in particular by fully digitizing the complex echo signal return, and using multiple parallel receiver channels for simultaneous measurements of signals from an array of spaced receiving antennas, it opened up new possibilities at the time for the measurement technique. It also set a new standard for improved electromagnetic compatibility with other services in the HF and MF spectrum.

Several of the original systems are still in use for ionospheric monitoring and research in different parts of the world. However these are aging, even though the original 1970's computers and digital hardware have been replaced by one or two new generations of technology. This has prompted the development<sup>4</sup> of the new system, described in this paper which has been designed to meet the same conceptual requirements. A prototype is now operating at the NASA Wallops Island Flight Facility.

## 2. Overall Description

Recent digital technology has made it possible to implement a coherent pulse transmitter and receiver system using digital signal processing [3]. The basic arrangement of the RF section is shown schematically in Figure 1 and is simply a digital implementation of the well known analog direct conversion architecture. The entire received signal spectrum, from 0.1 to 25 MHz, is low-pass Nyquist filtered and digitized to 14 bits at an 80 MHz sample rate. This data stream is then multiplied by numerically generated sinusoidal quadrature components at the desired receive frequency, and the resulting baseband components are decimated and low pass FIR filtered. This provides the desired receiver quadrature component output at a suitably reduced sampling rate, and for typical bandwidths, the processing gain gives 24-bit output resolution. For the transmitted pulse, an accurately timed quadrature component serial data stream is generated, and this is shaped by appropriate FIR low pass filters to a bandwidth-limited form. The filtered stream is then interpolated up to the 80 MHz clock frequency and up converted by multiplying with an identical numerically generated oscillator to provide the input to a high speed DAC. Coherence between transmitter and receiver is ensured by phase synchronization of the two numerical oscillators.

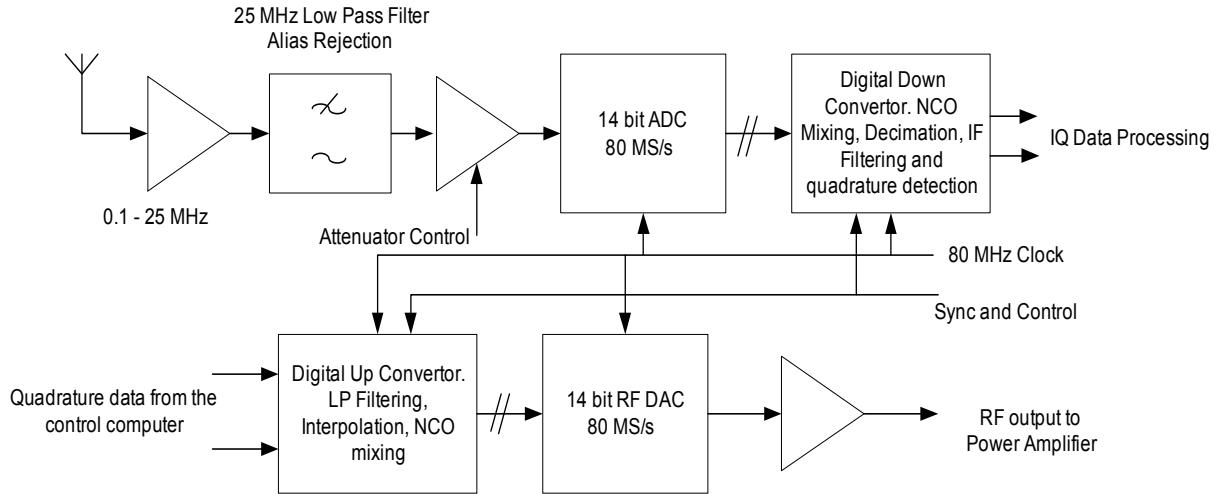


Figure 1. Digital HF Radar RF section, Simplified Block Diagram

The process of digital down conversion and up conversion is provided by a pair of commercially available single chip subsystems resulting in an extremely low component count implementation. This system can match or exceed the performance of an analog design of wide band frequency agile receiver with a dynamic range exceeding 100 dB. Furthermore the digital approach provides the important advantages of (1) exact phase and amplitude matching of the digital sections of multiple parallel receiver channels, and (2) the realization through the FIR filtering of a uniform group delay in the pass band to assure a stable phase measurement throughout the received pulse.

The analog portions of the system must be carefully designed so that they do not degrade the digital system performance. In particular, the amplification of the wide band signals from the receiving antennas before digital conversion must be linear enough to minimize spurious signal generation from the crowded HF spectrum. The Dynasonde application has traditionally used wide band dipole receiving antennas that work well in practice when spaced up to one quarter wave above the ground at the highest frequency of operation. Relative to loop type antennas the dipole has the advantage of being relatively less sensitive to local vertically polarized signals from AM broadcast transmitters. However, the dipole sensitivity to down coming signals necessarily falls with frequency due to its decreasing electrical height above ground.

A new very linear wide band dipole preamplifier has been developed for this system. For true wide band operation the dipole must be electrically short in length. NEC analysis of a dipole of overall length 4m shows a nearly uniform source impedance of just 20 pF from each element up to 10 MHz with the resistive term only becoming significant above 15 MHz. To provide a uniform coupling of the voltages induced across the dipole with frequency, the preamplifier must either present a very high impedance to preserve the response at low frequencies, or be in a charge sensitive configuration with capacitive feedback to the dipole terminals. The latter approach was selected because it has better noise performance and linearity.

The basic arrangement of the preamplifier is shown in Figure 2. Calibration can be conveniently coupled into the summing junctions with 1pF capacitors making it straightforward to relate the calibration to received signal strength, given that the dipole length and source capacitance are known.

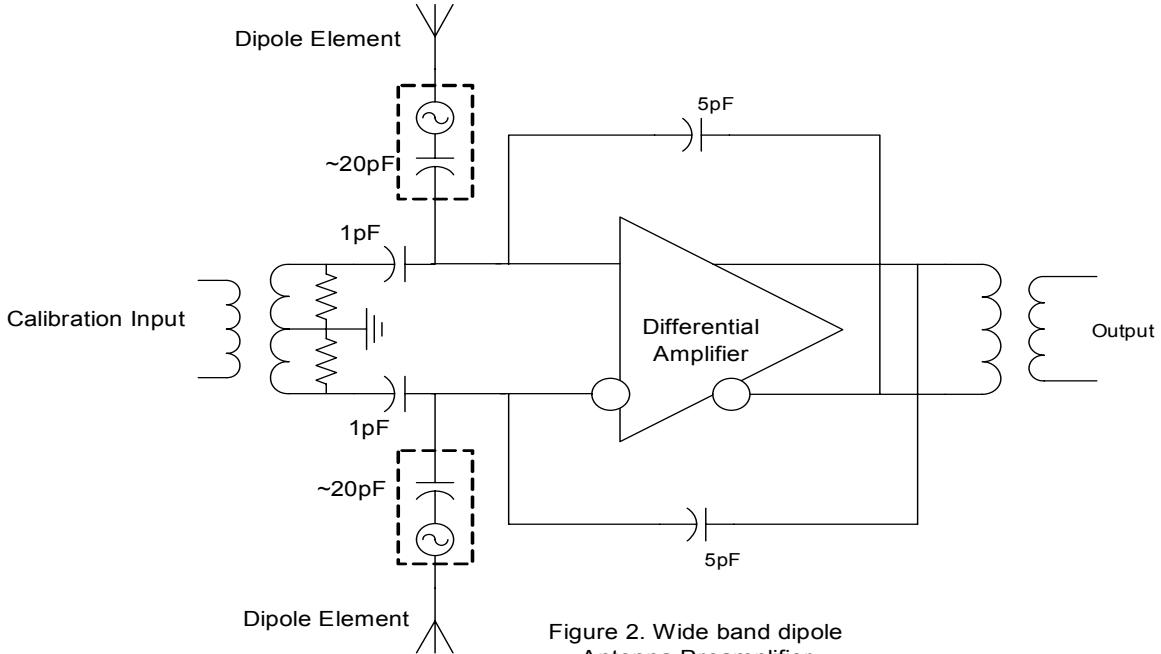


Figure 2. Wide band dipole Antenna Preamplifier

The preamplifier is realized with discrete semiconductors. A balanced JFET input stage is followed by a balanced cascode bipolar transistor output stage that is transformer coupled to the  $100\ \Omega$  balanced output. The performance achieved with this design is summarized in Table 1. Tests with the 4m dipole show the overall performance to be atmospheric noise limited over the whole frequency band at mid latitudes.

**Table 1. Preamplifier Performance**

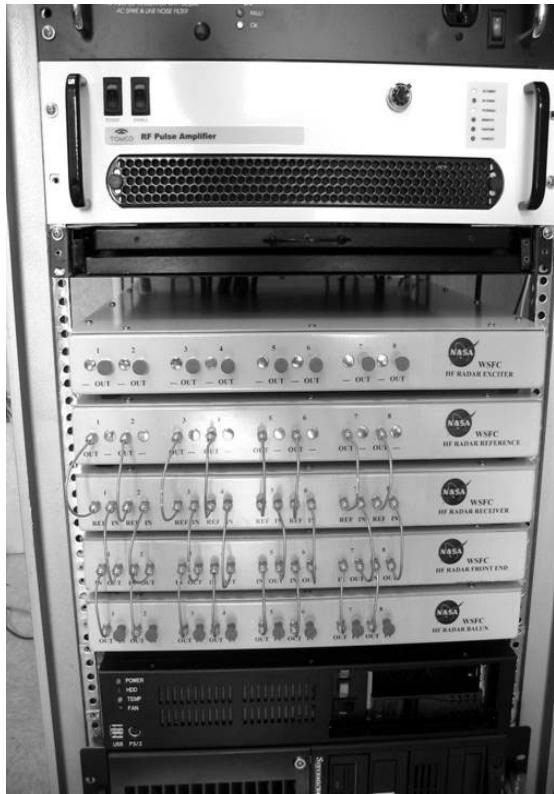
Frequency Response -3 dB 50 kHz to 28 MHz  
 Intercept point at 1 MHz. Third Order > +40 dBm, Second Order > +60 dBm  
 Intercept point at 10 MHz Third Order > +30 dBm, Second Order > +55 dBm  
 Common mode rejection 1 MHz > 50 dB, 10 MHz > 50 dB  
 Open circuit noise spectral density at 5 MHz < -148 dBm/Hz

The current radar system configuration allows for up to eight receive channels. The blanking and gain control for the input from each of the preamplifiers are managed using digital controlled attenuator and switches that exhibit a third order intercept of > +50 dBm. A balanced amplifier buffers the input to the ADC preceding the down conversion. Overall, the performance of all of the analog portions of the radar is well matched to the performance of the digital receiver stages that follow.

Physically the digital portions of the radar consist of four enclosures, a very low jitter 80 MHz reference, an eight-channel receiver, a two-channel exciter and the control computer. All reference signals are distributed to the receiver and exciter using fixed length  $50\ \Omega$  coaxial cables to assure maximum phase coherence throughout the system. The receiver and exciter enclosures are autonomous, that is they have their own timing state machines and tuning memories that are loaded prior to data collection. Exact synchronization of the two timing state machines is assured by distribution of a single universal time synchronized pulse from the GPS clock in the reference enclosure that is selected by the operator as the start time of a data collection.

USB-based microcontrollers are used throughout the system for communication with the control computer. Prior to data collection, multiple microcontrollers program the receiver and exciter microport control registers, store tuning words in memory, and program the state machine FPGA. Thus, all system control functions are pre-programmed prior to a sequence of data collection, and only need to be activated by the start pulse from the GPS. The system data multiplexer also uses a USB-core microcontroller and FPGA combination to multiplex and buffer up to 8 channels of data from the receiver chips, and to place those data in the USB endpoint buffer FIFO for

transmission to the control computer. Cumulative rates exceeding 1.2 M 16-bit complex samples per second are achievable with the multiplexer. Once the timing state machines have started a data collection, the only active USB traffic is the digital data traffic from the multiplexer endpoint FIFO to the control computer.



The timing controller in the exciter enclosure is also the source of the IQ serial sequence that forms the transmit pulse. Two deep memories for transmit and calibration waveforms are pre-programmed, and clocked out at particular times within the pulse repetition interval. The calibration pulse is generated within the sequence and fed to the preamplifiers in the field, but can also be switched into the analog input for tight loop calibration purposes.

The autonomy of the receiver and exciter also make it suited for bistatic operation. Two reference enclosures are required in that case. The internal GPS clock already assures exact (15 ns) timing synchronization of waveform and data collection. The only hardware change that would be necessary is that disciplined rubidium oscillators are required to replace the current 80 MHz OCXO.

The control computer that is provided with the system is a moderately high performance x86 system using Debian Linux as an operating system. All of the software for that CPU, and also for the various microcontrollers, is written in high-level C under Open Source licensing. The program directory hierarchy follows standard Unix traditions, and is ordered per system function so that a user can better understand how the system operates. The system can be fully remote controlled through a secure network interface.

Received raw IQ data files are available to the user through the network connection with the control computer at the sampling rate consistent with the system operational bandwidth (nominally 100 kHz). All the subsystem control parameters are recorded along with the data in the files as metadata to reduce any data interpretation ambiguities.

The system with 8 receive channels shown above can be housed in a 40 inch rack cabinet which also contains the 1 kW (optionally 4 kW) solid state class AB linear power amplifier at the top of the cabinet.

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### 3. References

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