An S-Band High Linearity Low Noise PHEMT MMIC Amplifier

M.Haridim, O.Rahmanony, D. Elad, J.Gavan

Department of Communication Engineering, HIT-Holon Institute of Technology
P.O. Box 305, Holon 58102, Israel
mharidim@hit.ac.il

Abstract
An S-Band high linearity and Low Noise PHEMT MMIC Amplifier for general application and WiMax band is demonstrated. This two-stage amplifier is designed to fully match for a 50 ohm input and output impedance. The amplifier has achieved 19dB small-signal gain, a noise figure of 1.3 dB, and a 24dBm 1-dB gain compression power. In addition, high linearity with 35dBm third-order intercept point and Recovery time of 50ns at the S-Band is achieved. The input and output return losses are 12 dB.

1. Introduction
Nowadays, wireless communication systems operate in a hostile jammer and blocking signal environment, this jammer signal degrade the receiver sensitivity due to the cross modulation distortion that is generated by the LNA nonlinearity and require exceptionally linear and Low noise receiver front-ends.

The emphasis of this work was to increase the dynamic range of the LNA, reduce the NF and increase the IP3 performance. The fully monolithic LNA presented in this paper achieves a noise figure below 1.3 dB at S-Band with a gain of 19 dB and high linearity with 35dBm third-order intercept point and recovery time of 50ns, using standard PHEMT 0.25um process.

2. Circuit Design
Choosing an active device will be the first and most crucial step in designing an LNA after major performance requirements such as NF, gain, return loss and IP3 are determined. Although some typical transistors are available in a typical PDK, they are often not optimized for the optimum LNA performance and different from design target. As such, an accurate set of device S and noise parameters for the optimum devices will be needed to design and predict the final LNA NF, gain, return loss and stability. The Noise and Small signal models for the optimized FET’s we used are shown in Figure 1[12][13][14]. The extraction of the parasitic parameters is done using the cold-FET method, and the intrinsic parameters are from hot-FET method. After optimizing these extracted parameters, the simulated S-parameters from the equivalent model are fitted to the measured data.

De-embedded two-port S-parameters of the PHEMT are measured by VNA HP8510C. After measuring 4 different FET devices (2F80um, 4F120um, 4F320um, 8F640um) the 8F640um FET was chosen to be implemented in the design. Different bias condition between the first and the second stage is needed in order to determine the NF and the output IP3 specification.

A schematic of the RF part of the LNA is shown in Fig. 2. The circuit consists of two common-source gain stages to provide enough power gain. The first and the second stage uses an on-chip inductive degeneration of the source to achieve a simultaneous noise and S11 match, and to improve RF stability.

\[
Z_{in} = s(L_s + L_o) + \frac{1}{sC_s} \left( \frac{V_{ds}}{C_{ds}} \right) I_v
\]

The load of the first stage, together with the DC block between the stages, is also used for inter-stage matching. The inter stage is using also as a frequency equalizer for flattening the desired band. The output of each stage is loaded with a band pass LC section to increase the gain at the desired Frequency and to isolate it from the other gain stage and from the external supply voltage.

The output matching which is designed to transfer maximum output power from the FET to the 50 ohm system. The first estimated were calculating according to the Cripps technique [15] the required optimum large-signal load impedance Zo is composed of Ropt and Cds.

Fig. 1 Noise and Small signal Model

Fig. 2 Simplified schematic of the LNA
The device was designed, network synthesized, simulated and optimized with the Agilent ADS, an optimization and EM simulation with momentum is performed to achieve the required circuit performance.

3. Measurements

The circuit was fabricated with a standard PHEMT 0.25um foundry process. Level 1 On-wafer measurements were performed using signal-ground signal probes. The chips were mounted in a ceramic package to investigate the influence of the bonding wires and the package parasitic and also to test the chips in extreme temperature environment. A 50 Ω test equipment for small signal parameters as N5230A PNA-L Network Analyzer and Spectrum Analyzer + Agilent 346B noise Source (Agilent E4440A) is used.

Fig. 4 describes the Gain measurement of the packaged LNA in ambient and extreme temperature conditions. In the ambient temperature the gain is about 19dB, +90 ºC degraded the gain in a 1dB.

Fig. 5 describes the Noise measurement of the packaged LNA in ambient and extreme temperature conditions. In the ambient temperature the NF is about 1.3dB, +90 ºC degraded the NF to 1.75dB

Fig. 6 and 7 describes the Input Return loss of the packaged LNA in extreme temperature conditions. In the ambient and extreme temperature the Input Return loss is less then -12dB.

Fig. 8 describes the Recovery time test of the packaged. The test performed in step of 10dBm input power to SSG. The setup recovery time is about 25nS. The recovery time of the device is less than 50nS.
4. Conclusions

An S-Band High Linearity Low Noise PHEMT MMIC Amplifier is presented. The amplifier has achieved 19dB small-signal gain, 1.3 dB of NF, 24dBm 1-dB gain compression power. In addition, high linearity with 35dBm third-order intercept point and recovery time of 50nS at frequency of S-Band is achieved. The input and output return loss 12 dB. The chip has been fabricated in a commercial GaAs PHEMT 0.25um foundry process.

Table 1 describe the Comparison of LNAs in the commercial market and this work.

<table>
<thead>
<tr>
<th>Product</th>
<th>Technology</th>
<th>Freq (GHz)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>Input RL (dBf)</th>
<th>GPS (dBm)</th>
<th>VDC (V)</th>
<th>Power Consumption (mW)</th>
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<tr>
<td>HMC102</td>
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<td>3.5-7</td>
<td>14</td>
<td>2.8</td>
<td>10</td>
<td>28</td>
<td>5V</td>
<td>250</td>
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<td>MGA 8670</td>
<td>GaAs</td>
<td>4</td>
<td>23.5</td>
<td>2</td>
<td>10</td>
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<td>80</td>
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<td><strong>This Work</strong></td>
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<td><strong>S-Band</strong></td>
<td><strong>19</strong></td>
<td><strong>1.3</strong></td>
<td><strong>12</strong></td>
<td><strong>34</strong></td>
<td><strong>5V/6V</strong></td>
<td><strong>440</strong></td>
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<td>MAX064-5</td>
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<td>18.8</td>
<td>5V</td>
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<tr>
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<td>22</td>
<td>5V</td>
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</tr>
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Table 1. Comparison of LNAs

5. References