A Low-Voltage Fully-Integrated 5GHz Low Noise Amplifier in 0.18μm CMOS

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Abstract

A 5GHz Low Noise Amplifier (LNA) is presented using the folded-cascode topology which is suitable for low-voltage Radio Frequency Identification (RFID) applications. It employs both NMOS and PMOS devices to reduce the required supply voltage to less than 1V. The circuit is fully integrated on-chip, with inductors implemented using stacked spirals to save space. It is experimentally demonstrated in 0.18μm CMOS and performs particularly well at 5GHz, with the noise figure being below 3dB. The gain and input 1dB compression point exceed 12dB and -11.5dBm respectively, while the input return loss is better than -20dB. The LNA has an active footprint of only 575μm by 525μm, and consumes less than 10mW from a 1V supply.

1. Introduction

The increasing demand for higher speed and longer range in Radio Frequency Identification (RFID) applications has recently motivated the industry to adopt new systems in the 5GHz band. As this highly competitive market constantly drives manufacturers to reduce costs, one promising solution is to integrate the RF front-end including the low noise amplifier (LNA) with existing digital CMOS circuits on the same chip.

Several LNA circuit topologies have been devised to yield a low noise figure and high gain [1, 2]. Most of the designs reported in the literature are based on the conventional cascode structure, which employs two NMOS transistors stacked between the supply rails and thus requires a high voltage [3-6]. Its operation with a low voltage below 1V is problematic, especially for less expensive and more mature CMOS technology nodes such as 0.25μm and 0.18μm [7]. More recently, a few publications have shown that the folded-cascode topology is more suitable for low supply voltages [8-10]. This structure utilizes the complementary nature of CMOS, employing both NMOS and PMOS transistors to reduce the required voltage. However the work conducted thus far has suffered from low linearity [10], high input reflection coefficient or high power consumption [9].

In this paper, a folded-cascode LNA suitable for low-voltage, low-power RFID active tags and readers is demonstrated using a well-balanced design approach that yields a competitive noise figure and gain, a high linearity and a good input match. The circuit is fully integrated on-chip, with inductors implemented using stacked spirals to minimize footprint and cost. It is experimentally demonstrated in a standard 0.18μm CMOS process showing very good performance at 5GHz. A low noise figure of less than 3dB is achieved, while the gain and input 1dB compression point exceed 12dB and -11.5dBm. The input of LNA is also well matched with the return loss being better than -20dB. The integrated circuit (IC) measures 700μm by 600μm with an active area of only 575μm by 525μm, and consumes less than 10mW from 1V.

2. Circuit Architecture and Design

A circuit schematic of the folded-cascode LNA [8] is shown in Fig. 1. It consists of a common-source NMOS transistor (M_1) that provides the transconductance g_m of the LNA, followed by a common-gate PMOS transistor (M_2) that acts as a current buffer to reduce the miller effect, improve the high frequency response and increase the reverse isolation. Due to the complementary operation of the PMOS transistor, the supply voltage V_{DD} is connected to its source between the two devices that now appear in parallel. Thus the supply voltage V_{DD} only needs to be greater than the gate-to-source overdrive voltage of M_1. This is in contrast to the conventional cascode structure, where M_2 is also an NMOS device stacked on top of M_1 in series, which increases the supply voltage requirement to be at least twice the gate-to-source overdrive. Therefore this circuit is more suitable for low-voltage applications below 1V, as conventional architectures would typically require 1.8V or more in 0.18μm CMOS technology. A comparative reduction in supply voltage is also expected for newer technology nodes such as 90nm or 65nm.

Several performance metrics need to be considered at the same time when designing an LNA, including noise figure, gain, linearity, input match and power consumption. The main objective of this design is to achieve a noise figure of less than 4dB at 5GHz, while optimizing the remaining parameters as much as possible.

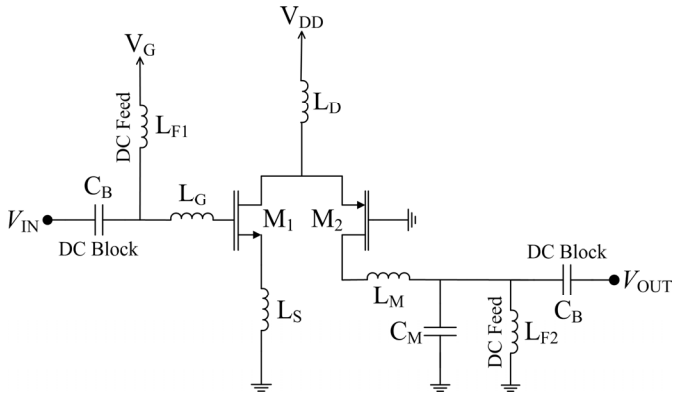

Fig. 1: Circuit schematic of the folded cascode LNA.

Noise and impedance matching at the input of the LNA are essential to minimize the noise figure and increase gain. This can be simultaneously achieved by using inductive degeneration at the source of transistor M_1 (L_S), followed by series resonance at its gate (L_G), as shown in Fig. 1. The input impedance Z_{IN} in this case is approximately given by:

$$Z_{IN} \approx j\omega L_G - \frac{j}{\omega C_{gs}} + j\omega L_S + \frac{g_m L_S}{C_{gs}}, \tag{1}$$

where L_G is the gate inductor, C_{gs} is the gate-to-source parasitic capacitance, g_m is the transconductance of M_1 and L_S is the source inductor. As the gate contributes much less noise than the drain-to-source channel, especially for a double-connected multiple-finger gate with the finger width minimized to 1.5µm, its contribution to the noise figure can be neglected. In this case, the noise factor F can be approximated as [11]:

$$F \approx 1 + \frac{\overline{i_{nd}^2}}{\overline{i_s^2}} \frac{\omega^2 C_{gs}^2}{g_m^2} \left| 1 + \left(j\omega L_G - \frac{j}{\omega C_{gs}} + j\omega L_S \right) Y_s \right|^2, \tag{2}$$

where i_{nd} is the drain noise current, i_s is the source noise current and Y_s is the source admittance 1/50Ω. From (1) and (2), simultaneous impedance and noise matching can be accomplished if:

$$j\omega L_G - \frac{j}{\omega C_{gs}} + j\omega L_S \approx 0, \quad \frac{g_m L_S}{C_{gs}} \approx 50\Omega. \tag{3}$$

The inductor L_D is designed to resonate at 5GHz with the total parasitic capacitance seen at the drain of M_1 and source of M_2, presenting a high impedance branch for the signal current and forcing most of it to flow into M_2. This improves the gain and noise figure of the LNA [3]. The output of the LNA can then be impedance matched to the 50Ω load for maximum gain, which is achieved at 5GHz using an inductor-capacitor network (L_M and C_M) as shown in Fig. 1. The inductor L_{F2} provides a feed to ground for the DC current of M_2.

All passives in this design are fully integrated on-chip. Inductors are implemented using spirals in the top two metal layers, which are connected in series and vertically stacked to save space [12]. The mutual inductance between the two spirals contributes significantly to the overall inductance of the structure, causing it to be about four times than that of one of the spirals. Therefore the spiral size required for a given inductance is much smaller [12]. Where a relatively higher quality factor (Q) is necessary for better performance however, a hollow spiral is constructed with a few inner turns removed as they add parasitic resistance but contribute little to inductance [13]. Capacitors are implemented using metal-insulator-metal (MIM) structures, which provide a high Q at a reasonable capacitance density. Furthermore, a thicker top metal layer is used to minimize conductive losses and improve performance.

3. Experimental Results

The LNA was fabricated in a standard (six-metal, single-poly) 0.18μm CMOS process. A photograph of the IC is shown in Fig. 2. It occupies a total die area of 700×600μm^2 including bonding pads and the active circuit area is 575×525μm^2. The circuit consumes less than 10mA of current from a 1V voltage supply.

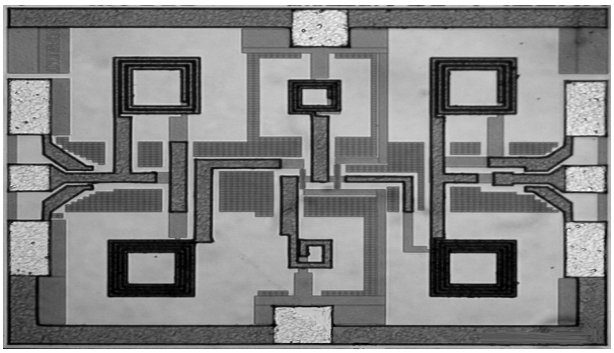

Fig. 2: Photograph of the LNA IC.

A direct on-wafer measurement of the IC was carried out using co-planar RF probes and DC probes. Fig. 3(a) shows the input and output reflection coefficients $|S_{11}|$ and $|S_{22}|$ of the LNA. As depicted from the plot, the input and output return loss are less than -23.1dB and -11.7dB respectively around 5GHz. Fig. 3(b) shows the forward transmission $|S_{21}|$ and noise figure (NF) of the amplifier. The gain is higher than 12.6dB and the noise figure is about 3dB at 5GHz. The amplifier's linearity was also tested and the input 1dB compression point (P_{1dB}) is higher than -11.5dBm.

Table 1 summarizes this work's performance in comparison with five other LNAs in the 5GHz band: [5-7, 9, 10]. It is clear that our LNA is better than most in terms of size, supply voltage and power consumption, making it more suitable for portable wireless devices. In [5, 9, 10], a low noise figure is only attained at the expense of DC power, input match, gain or linearity. This is in contrast to this LNA where a good balance between performance metrics is achieved. Moreover some of the other designs rely on higher-quality off-chip components [6] or on postprocessing of the measured data [7].

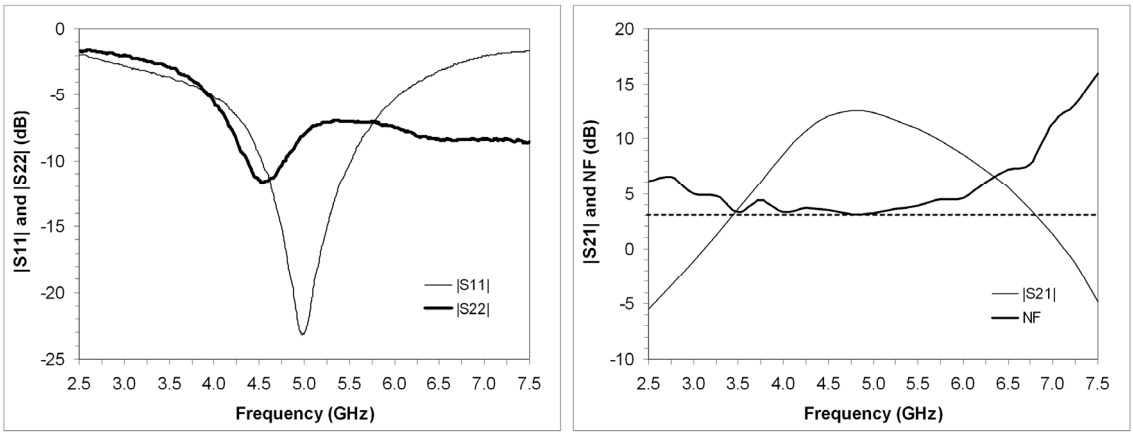

Fig. 3: (a) LNA input $|S_{11}|$ and output $|S_{22}|$ reflection coefficients and (b) LNA gain $|S_{21}|$ and noise figure NF.

4. Conclusion

A fully-integrated LNA suitable for low-voltage 5GHz applications has been developed using standard 0.18μm CMOS technology. It employs both NMOS and PMOS devices in a folded cascode configuration to reduce the supply voltage to 1V. Experimental results were demonstrated showing good performance at 5GHz

compared to other work. The LNA occupies an area of 575×525μm^2 and consumes less than 10mW from a 1V supply.

Table 1: Summary of LNA's characteristics compared to other work.

	CMOS Node	Area	DC Power	Center Freq.	Input Match	Gain $\|S_{21}\|$	NF	P_{1dB}
[5]	0.25μm	500×795μm^2	10mW at 2V	5.2GHz	-30dB	10dB	3.0dB	-8.3dBm
[6]	0.18μm	830×830μm^2	10.4mW at 1.8V	5.25GHz	-15.9dB	16.1dB	2.2dB	-13.6dBm
[7]	0.18μm	400×600μm^2	16mW at 1V	5.75GHz	—	14.2dB	0.9dB	—
[9]	0.18μm	900×800μm^2	22.2mW at 1V	5.8GHz	-5.3dB	13.2dB	2.5dB	–14dBm
[10]	90nm	754×720μm^2	11.1mW at 1V	5.5GHz	-12.7dB	15.0dB	2.8dB	-17.9dBm
This work	0.18μm	575×525μm^2	10mW at 1V	5.0GHz	-23.1dB	12.6dB	3.0dB	-11.5dBm

5. References

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