Serial DataPath Implementation on a Xilinx Spartan 3 FPGA For Global Positioning System

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Abstract

This paper presents a hardware design of a serial DataPath that can be used in GPS (Global Positioning System) architecture. Field Programmable Gate Arrays (FPGAs) are used for the hardware implementation part of the design. The implemented DataPath is for a simple Reduced Instruction Set Computer (RISC) that has been built using VHDL (VHSIC Hardware Description Language) and simulated using ModelSim XE II 5.6e. The hardware part of the design was done using Digilent Spartan 3 starter kits that are used for a rapid digital circuit implementation.

Keywords: FPGA, GPS, VHDL, RISC.

1. Introduction

Global Positioning System (GPS) is a worldwide radio-navigation system formed from a constellation of twenty-four satellites and their ground stations. The satellites are transmitting information about their location and time continuously [1, 2, and 3]. The system uses these satellites as reference points to calculate positions accurate to a matter of meters. A GPS receiver operates by measuring its distance from each of the visible satellites. GPS receiver is available with serial communications or USB ports [4, 5, and 6].

In this paper a DataPath with serial communication port has been designed using Hardware Description Language (HDL), and implemented in hardware using Field Programmable Gate Arrays (FPGAs). The implemented DataPath with the serial communication port are suitable for the design of Global Positioning System using VHDL. The UART (Universal Asynchronous Receiver Transmitter) part of the design was also built using VHDL and implemented in FPGA. The design has been synthesized and implemented using Xilinx ISE 6.2i tools, and simulated using ModelSim XE II 5.6e, at the end the design has targeted a Xilinx Spartan XC3S200FT256 FPGA.

2. System Hardware

The hardware of the system design mainly consists of the DataPath part and the UART (Universal Asynchronous Receiver Transmitter) part that will be connected to any serial communication device. The main goal of this work is to use the implemented DataPath and connected UART for the application of Global Positioning System [7 and 8]. The UART and DataPath were designed and downloaded on FPGA chip [9], and then tested with serial communication port of the PC as shown in Figure 1.

3. DataPath Implementation

The DataPath has been implemented on Digilent Spartan 3 development Board, and some operations have been tested on the 7-segment and LEDs of the kit [10 and 11]. The development kit has four 7-segments and 8 LEDs, the 7-segments have been used for testing the arithmetic operations, whereas the logic operations have been tested using the 8 LEDs. A multiplexing between the four 7-segments has been made using VHDL with a clock of 1KHz. The generated Register Transfer Level (RTL) Schematic is shown in Figure 2, the design has been tested for different instructions and verified the correctness of the system.
Figure (1) System Hardware

Figure (2) Register Transfer Level Schematic Circuit
<table>
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<tr>
<th>Figure (3) OR Instruction</th>
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<tr>
<td>Figure (4) NEG Instruction</td>
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<td>Figure (5) SHR Instruction</td>
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<td>Figure (6) SHL Instruction</td>
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<td>Figure (7) SHA Instruction</td>
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4. Conclusion and Future Work

A hardware design of a DataPath that deals with data in a serial manner has been implemented, such that it can be used for Global Positioning System, with UART communication port. The system was designed using VHDL in a high level design method. All parts of the design have been simulated and implemented using Xilinx tools. Spartan 3 FPGA with 256 input/output pins and 200K logic gates has been used as a target technology. The system was tested in both simulation level using ModelSim and hardware level using Digilent Spartan 3 development board. The UART part of the design has been test with the serial communication port of the personal computer for different data rate. More developments are needed to build a complete Global Positioning System on a Field Programmable Gate Array. This development includes building a core RISC processor that will be used in building the GPS system.

References

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