Impact of Multi-Layered Gate Design on Hot Carrier Reliability of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET

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Abstract

The paper discusses hot carrier reliability assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET involving channel recession and gate electrode workfunction engineering integration onto the conventional MOSFET, using ATLAS device simulator. Further, the impact of gate stack architecture on the device reliability of GEWE-RC MOSFET is studied in terms of hot carrier behavior. TCAD simulations reveal reduction in the hot carrier reliability metrics such as electron velocity, electron temperature, conduction band offset, hot electron injected gate current and impact ionization substrate current.

1. Introduction

For the last few decades, Si CMOS technology has been driven by device scaling to increase performance, as well as reduce cost and maintain low power consumption. A paradigm shift has been occurring in the industry, where materials innovation, rather than scaling, is becoming the primary enabler for performance enhancement in CMOS technology. A critical challenge for the microelectronics industry is the need for higher permittivity dielectrics (High-K) to replace silicon dioxide in order to reduce the gate leakage current. The MOSFET gate oxide thickness is rapidly approaching the direct tunneling limit that ultimately leads to intolerably increased standby power [1] and/or impractical applications [2]. Thus, accurate characterization and simulation of ultra-thin oxides in the direct tunneling regime is essential and crucial.

Further, to achieve higher speeds and higher packing densities, gate length miniaturization is the key parameter, but it leads to short channel effects (SCEs) and hot carrier effects. Recessed Channel (RC) MOSFET [3-4], due to the presence of a groove between the source and drain regions, are considered as promising candidates that provides excellent hot carrier effect immunity, DIBL and punchthrough suppression; thereby enhancing the electrical and switching characteristics. But at the same time, owing to the groove separating the source and the drain regions, the threshold voltage, \( V_{th} \), and the driving current performance deteriorates. So, in order to enhance these characteristics, GEWE architecture, implementing the dual material gate design [5-6], is taken into account. In GEWE architecture, the gate metal is made up of two different materials with different workfunctions; thereby introducing a step in the channel potential profile. The GEWE structure [7], thus, achieves simultaneous suppression of SCEs and driving current enhancement owing to the perceivable step in the channel potential profile and a more uniform electric field distribution along the channel. Multi-Layered Gate Electrode Workfunction Engineered Recessed Channel (MLGEWE-RC) design, considered in this study (Fig.1), thus, integrates the advantages of RC MOSFET with multi-layered-gate [8-9] and GEWE architecture implementing the dual material gate design; and is of paramount importance in nanoscale devices.

2. Device Manufacturing Feasibility

As predicted by the device designers, device performance deterioration becomes a stringent limitation as the devices are scaled down to Sub-50nm regime. Hence, in order to improve and enhance the lifespan of conventionally scaled MOSFET designs, various designs are approaching the device realization scenario. Although MLGEWE-RC MOSFET (Fig.1) has not yet been fabricated, the design has been proposed with an optimistic fabrication outlook.

Various fabrication techniques of grooved gate/recessed channel MOSFETs [10-11] and multi-layered gate dielectric architecture [12] have been reported in the literature. Further, several integration schemes for workfunction
engineered gate electrodes have already been suggested in past such as tilt angle evaporation metal gate deposition [5], metal interdiffusion process [13] and fully silicided metal gate [14].

3. Hot Carrier Reliability Evaluation

For the prediction of device performance and for the optimization of MOS devices, the hot carrier degradation effects are of paramount importance [15]. Aggressive scaling of the gate lengths has rendered hot carrier injection induced performance degradation of MOSFETs. Further, as MOSFET dimensions shrinks to sub-50 nm regime, Drain Induced Barrier Lowering (DIBL), becomes more prominent. DIBL effect is found to be more pronounced in RC devices (Barrier Lowering, $\Delta \Psi_{RC}=40mV$) in comparison to GEWE-RC as is clear from Fig.2, having $\Delta \Psi_{GEWE}=25mV$ resulting in a higher electrostatic coupling. Significant barrier lowering in RC leads to leakage current (due to drain bias) [4] just below the gate and hence can result in increased power dissipation. However, GEWE-RC MOSFET exhibits step conduction band energy profile in the channel due to metal gate workfunction difference. This screens the region near the source from the drain bias variations and hence, accounts for lowest DIBL, showing better control of SCEs over RC MOSFET. Simulation results [16] also reflect the impact of multi-layered gate stack architecture on device performance of GEWE-RC MOSFET, resulting in a new structure termed as MLGEWE-RC MOSFET (Fig.1). As is clear from the results, the screening of the channel region from drain bias variations is tremendously increased with the gate stack architecture. With MLGEWE-RC, due to improved gate controllability over the channel, DIBL is significantly lowered resulting in $\Delta \Psi_{MLGEWE}=19mV$.

Fig.1. Schematic cross-sectional view of MLGEWE-RC MOSFET designs. Design Parameters are stated as Channel Length ($L_G=L_{G1}+L_{G2}$) = 50 nm, $L_{G1}$=$L_{G2}$= 25nm, Device Width (W) =1μm, Groove Depth, (d)=80nm, $X_1$=74nm, NJD=10nm, $N_D$=1x10$^{20}$ cm$^{-3}$, Source/Drain Doping, $N_p$=1x10$^{20}$ cm$^{-3}$, $t_{ox1}=t_{ox2}$ =2nm, $t_{ox}$=4nm, $\varepsilon_{ox}=\varepsilon_{ox1}$ 3.9, $\varepsilon_{ox2}$=10, Effective Oxide Thickness, $EOT=t_{ox1}+\frac{\varepsilon_{ox1}}{\varepsilon_{ox2}}t_{ox2}$, $V_{SUB}=0V$ and $V_{DS}=1.0V$; unless otherwise specified. Work function ($\Phi_{M1}$) = 4.77V for RC and for GEWE-RC and MLGEWE-RC, ($\Phi_{M1}$) = 4.77V and ($\Phi_{M2}$) = 4.10V. $V_{DS}=0.0V$ and $V_{DS}=0.5V$; unless otherwise specified. Work function ($\Phi_{M1}$) = 4.77V for RC and for GEWE-RC and MLGEWE-RC, ($\Phi_{M1}$) = 4.77V and ($\Phi_{M2}$) = 4.10V.

Fig.2. Conduction band energy variation along the channel at a depth of 1nm below Si/SiO$_2$ interface for $V_{GSS}=0V$ for MLGEWE-RC, GEWE-RC and RC devices at $V_{DS}=0.5V$ and 1.0V.

Fig.3 predicts the electron velocity variation of RC, GEWE-RC and MLGEWE-RC MOSFET designs, with the normalized position along the channel respectively. In order to improve the carrier injection i.e. carrier transport efficiency in the channel, electron velocity near the source should be more than near the drain. Significantly higher electron velocity (3.2x10$^7$ cm/sec) near the source side is obtained for GEWE-RC in contrast to 0.8x10$^7$ cm/sec and obtained for RC MOSFET as is clear from Fig.3; thereby enhancing the source carrier injection appreciably into the channel. Moreover, incorporating the multi-layered gate architecture on GEWE-RC MOSFETs results in a significant improvement in the electron velocity near the source (1.08x10$^7$ cm/sec for MLGEWE-RC); due to improved gate controllability over the channel; hence leading to higher carrier transport efficiency and current driving capability. Further, Fig.3 also demonstrates that a lower electron velocity of 0.04x10$^7$ cm/sec near the drain end is obtained for MLGEWE-RC MOSFET in contrast to 1.3x10$^7$ cm/sec and 2.1x10$^7$ cm/sec observed for GEWE-RC and RC respectively, providing excellent hot carrier immunity. Fig.4 predicts the electron temperature variation of RC, GEWE-RC and MLGEWE-RC MOSFET designs, with the normalized position along the channel respectively. The electron temperature gradient i.e. $\delta T/\delta (x/L)$ as the carriers move from source to drain is reduced significantly with GEWE-RC MOSFET design in comparison to the RC MOSFET. $\delta T/\delta (x/L)$, as evaluated 10% away from the drain towards the source, gives a remarkable reduction in electron temperature to 1290K in GEWE-RC MOSFET from 6480K in RC as is
clear from Fig.4 respectively. Due to the corners present in the recessed channel structure, the electron temperature also falls down abruptly at the corners; thereby significantly enhancing the hot carrier immunity of the device. Fig.4 also predicts the impact of multi-layered gate architecture on the electron temperature of RC and GEWE-RC MOSFETs. As is clear from the results, an appreciable reduction in the electron temperature gradient for MLGEWE-RC ($\delta T/\delta x/L=160K$) is obtained due to improved gate control over the channel; thus proving excellent hot carrier reliability of the device.

For system-on-chip and high-speed logic applications, device degradation is mainly attributed to the existence of impact ionization substrate current (II-I$_{\text{SUB}}$) and hot electron injected gate current (HE-I$_{\text{G}}$). The hot carrier injection gate current and the impact ionization substrate current accurately reflects the hot-carrier-effect reliability and hence, used as the hot carrier reliability indices. During the study on the gate current, we have adopted the hot electron injection model and for the substrate current simulations, impact ionization model was considered. Fig.5 depicts that HE-I$_{\text{G}}$ in GEWE-RC MOSFET is reduced significantly in comparison to RC MOSFET. The main factor resulting in the smaller hot carrier effects in RC devices is the corner effects. When the carriers move across the channel from source to drain, they have to surmount the potential barriers formed at the two corners. HE-I$_{\text{G}}$ in RC devices is appreciably reduced consequentially. Fig.5 also explains the impact of multi-layered gate architecture on HE-I$_{\text{G}}$. MLGEWE-RC MOSFET designs exhibit significantly reduced HE-I$_{\text{G}}$ due to higher gate control over the channel. Fig.6 explains the II-I$_{\text{SUB}}$ in RC, GEWE-RC and MLGEWE-RC MOSFETs. MLGEWE-RC MOSFET design exhibit appreciably reduced II-I$_{\text{SUB}}$ due to higher gate control over the channel; resulting in improved current driving capability and lower leakages. For low-voltage analog circuit applications, low II-I$_{\text{SUB}}$. HE-I$_{\text{G}}$ and lower electron velocity and temperature near the drain end are important design parameters.
5. Conclusion

In this paper, we emphasize our focus on multi-layered gate design, gate electrode workfunction engineering and recessed channel architecture incorporation onto the conventional bulk MOSFET for improved hot carrier reliability of scaled MOS devices. The performance enhancement in MLGEWE-RC MOSFET is through enhanced gate control that increases the device immunity to short channel and hot carrier effects. Further, the reduction in hot electron injected gate current; electron velocity and electron temperature near the drain end; and impact ionization substrate current; is achieved with MLGEWE-RC MOSFET; thereby, enhancing the hot carrier reliability of the device. The work, thus, presents MLGEWE-RC MOSFET design as a promising solution for realizing CMOS technology in wireless; and high performance applications where device and hot carrier reliability is a major concern.

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7. References