Grounded guard tracks placed adjacent to transmission line interconnects can change their impedance significantly. We report closed-form expressions for line capacitance and impedance of transmission line interconnects with adjacent guard tracks. Results are validated by finite-difference time-domain (FDTD) simulations and measurements. The proposed results can have significant impact on the analysis of coupled interconnect lines, where the use of these grounded tracks is a common design practice.

1. Introduction

Grounded guard tracks adjacent to transmission line interconnects are often used for reduction of crosstalk in a variety of routing topologies [1] and high-speed mixed signal systems [2-5]. While full-wave spectral domain analysis for crosstalk reduction using additional ground tracks has been discussed in detail [6], the effect of such ground tracks on the impedance of the interconnect line itself is usually lost sight of. From system design consideration an accurate design formula for the impedance of such interconnects is of substantial practical use. With the introduction of grounded guard tracks, the line impedance becomes a function of the separation between the line and ground tracks, in addition to the interconnect line width, height of the substrate and the dielectric constant of the substrate. In this work, we report closed-form expressions for the capacitance and impedance of transmission line interconnects with adjacent guard tracks using variational technique combined with transverse transmission line technique [7], which offers a relatively simple approach for the solution of such type of problems. The design methodology presented in this paper can aid designers to strategically place guard tracks, thereby ensuring lower crosstalk and superior signal integrity. It may be mentioned that the structure under discussion has useful application in reducing crosstalk between interconnect lines in multichip modules carrying high-speed signals and is different from coplanar stripline structures which do not have a bottom ground plane.

Out of all the analytical methods, the variational method treats the dielectric boundary conditions in a generalized way. Thus it is possible to analyze multilayer microstrip lines also without much difficulty. The accuracy of this method is insensitive to the choice of the trial function. Thus it is possible to take into account all the dielectric boundary conditions no matter how many planar boundaries exist in these lines [8]. The method is based on the calculation of the line capacitance by the static field theory, and, therefore it is an approximation to the EM theory. Unlike conformal mapping and other analytical techniques – which are also the static field theory – the analytical treatment of multiple boundaries is easier by the variational method [7-9]. The computational time is also far lesser than other techniques. All of this makes the variational method combined with the transverse transmission line technique a natural choice for analysis of the interconnect structures in our paper. The analytical model has been verified both by field simulator and measurements performed on specially designed PCB interconnect tracks.

2. Analytical Model

Fig. 1 shows the cross-section of the interconnect line which is at the centre over a ground plane at the bottom and resembles a standard microstrip-like structure. In order that the interconnect line carrying signal is isolated, grounded metallic traces have been placed on both sides of the line. The interconnect line is assumed to be very thin having a width ‘w’. The thickness of the dielectric (lower region) is $b_2$ having a permittivity $\varepsilon_2$. The ground tracks, coplanar with the interconnect line, has a separation ‘d’ from the line on both sides. The interconnect line, therefore, sees grounded planes both below vertically and sideways laterally.
The standard technique for determining line capacitance is explained in detail in [7] and hence only salient steps leading to the variational formula for the capacitance are presented here. The variational expression for the capacitance of a multilayer structure, as shown in Fig. 1, is given by:

\[
C = \sum_n \left[ \frac{(1 + 0.25A)^2}{(L_n + AM_n)^2} \right] P_n / Y
\]

where

\[
L_n = \sin(\beta_n w/2)
\]

\[
M_n = (2/\beta_n w)^3 \left[ \frac{3(\beta_n w/2)^2 - 2\cos(\beta_n w/2) + (\beta_n w/2)^2}{2} \right] \sin(\beta_n w/2) + 6
\]

\[
P_n = (2/n\pi)(2/\beta_n w)^2
\]

\[
\beta_n = n\pi / c
\]

\[
A = \sum_{n \text{ odd}} \left[ \frac{(L_n - 4M_n) L_n P_n}{Y} \right]
\]

\[
Y_{\text{lower},n} = \varepsilon_0 \varepsilon_2 \coth(\beta_n b_2)
\]

\[
\beta_n = n\pi / c
\]

\[
c = 2d + w
\]

Note that in equation (1) the only parameter that needs to be determined is the admittance \(Y\) at the charge plane \(y = y_0\). To compute the admittance \(Y\), we take shield walls (both lateral and top) in the upper region at very large distance to simulate open boundary conditions of an open microstrip structure and electric walls in the specified physical distance in the lower region. The admittance of the lower region in Fig. 1 is given by

\[
Y_{\text{lower},n} = \varepsilon_0 \varepsilon_2 \coth(\beta_n b_2)
\]

where, \(\varepsilon_2\) and \(b_2\) is the permittivity and height of the dielectric layer, respectively, and is computed for odd values of \(n\) excluding \(n = 0\). The distance \(c\) is shown by dotted lines. The admittance of the upper region in Fig. 1 is given by
\[ Y_{Upper,n} = \varepsilon_0 \varepsilon_3 \coth(\beta_n b_3) \]
\[ \beta_n = n \pi \sqrt{c'} \]
\[ c' \gg w \]
\[ b_3 \gg b_2 \]  

(3)

where, \( \varepsilon_3 \) and \( b_3 \) is the permittivity and height of the dielectric layer (upper region) respectively and is computed for even values of \( n \) excluding \( n = 0 \). Substituting equations (2) and (3) in (1), we compute the line capacitance for these two regions; \( C_{Lower} \) and \( C_{Upper} \), respectively.

The proposed design model is versatile and can qualitatively be used to analyze microstrip lines also. It can be seen as the separation ‘\( d \)’ increases, the admittance parameter \( Y_{Lower} \) modifies and formulation given above reduces to the basic microstrip formulation. The results are valid for a range of dielectric substances. The results obtained in this paper are accurate up to 5 - 7 GHz, which incidentally happens to be the frequency of interest in current high-speed interconnects. If the interconnect has a small but finite thickness ‘\( t \)’, equation (1) can still be used by replacing \( Y \) in equations (2) and (3) by \( Y/h (\beta_n t) \) as reported in [7-10]. The expression for \( h (\beta_n t) \) for the structure considered is given by

\[ h(\beta_n, t) = \frac{1}{2} \left[ 1 + \frac{\sinh\{\beta_n(b_2 - t)\}}{\sinh\{\beta_n b_2\}} \right] \]  

(4)

From the expression of characteristic impedance for a microstrip line [9], the impedance \( Z \) of the interconnect structure can now be computed as

\[ Z = \frac{1}{\sqrt{\sqrt{(C_{Lower} + C_{Upper})(C_{Lower} + C_{Upper})}}} \]

(5)

3. Results

Results obtained from the above discussion are compared with FDTD simulations to check their accuracy. Fig. 2 gives a comparative plot of the characteristic impedance of an interconnect line with adjacent grounded guard tracks for a range of dielectric substrates (\( \varepsilon_r = 2.2, 4.6, \text{and} 9.9 \)).
It is interesting to know that the characteristic impedance $Z$ reduces substantially when the ground tracks are placed close to the line interconnects. The introduction of guard tracks close to the interconnect line results in increase in the lateral capacitance between the line and the guard tracks. This reduces the characteristic impedance of the interconnect line. The results are validated by measurements performed on fabricated interconnect structures of different specifications, using vector network analyzer and are highlighted in Fig. 2. The theoretical results show good agreement with the measured data, which validates our analysis. As the distance between the line and the ground tracks increases, the characteristic impedance $Z$ settles to a final value, which corresponds to that of a microstrip line. These values corroborate to the microstrip line impedance obtained from Wheeler’s equation [10].

4. Conclusion

While the use of ground tracks is reported for crosstalk alleviation, its effect on the line impedance has not been reported so far. We propose a fast and efficient design methodology for computation of line impedance of a transmission line interconnect with adjacent grounded guard tracks. The proposed analysis highlights the effect of ground tracks on line impedance. The design methodology can be applied to ensure superior signal integrity in dense routing topologies and coupled interconnects where ground tracks are commonly used to avoid crosstalk. It may be mentioned that though the present work is concerned with the effect of ground tracks on the impedance of interconnect lines; the analysis can be used for crosstalk related performance evaluation of coupled interconnect lines also.

References


