

Quarter-Circle Shaped Plane Cavity Resonator for Skew-Free and Low Jitter Clock Distribution Network

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Abstract

This paper proposes a quarter-circle shaped plane resonator for skew-free and low jitter clock distribution network (CDN). A cavity resonator consists of the embedded planes in a package or PCB and an inductive load. The resonant frequency can be controlled by the inductance of the load and quarter-circle shaped plane can make all edge having the same phase and also same amplitude. We have successfully demonstrated a 1.35 GHz clock delivery network with a skew of 0.5 ps, and suppressed jitter through modeling and simulation.

1. Introduction

In a high-speed synchronous ICs, it is critical to minimize timing uncertainties of the clock signal, because the clock signal has a significant role to provide a reference for data interfaces and all circuit blocks. In order to distribute the clock signals to the entire silicon ICs, global on-chip interconnections are normally used. However, multiple cascaded repeaters should be inserted into the on-chip interconnections, to decrease the loss and delay of the on-chip interconnections. It is hard to isolate the power and ground of the cascaded repeaters from other power supply networks of noisy digital logic blocks, since the clock should be distributed the entire chip. Hence, the cascaded repeaters can be sources of significant jitter and skew problems affected by the power supply switching noise generated by the digital logic blocks [1], [2]. Furthermore, the latency goes up in an H-tree structure of on-chip clock distribution network, to match the length of the clock source to every destination. A hybrid clock distribution scheme is proposed using a package substrate, which provides less resistance and capacitance of interconnections than those of on-chip interconnects [3]. The hybrid clock distribution scheme is able to remove the effect of simultaneous switching noise (SSN) on the clock signal delivery through interconnections of package layers. However if the clock source signal has an amount of jitter, distributed signals have also a lot of jitter. There are various resonant techniques to achieve a multi-GHz clock distribution with low skew and jitter, such as a standing-wave oscillator and a coupled transmission line [4], [5]. However the resonant techniques are limited to high frequencies by the size of on-chip transmission lines. Furthermore, the integration of a high Q resonance is not easy with the process of silicon substrate. This paper proposes an off-chip standing wave resonator for on-chip clock distribution, which is consist of a package plane and an inductive load. The structure of a circular shaped plane is proposed to implement skew-free clock delivery network. We successfully demonstrate time-domain and frequency-domain simulation results including the excitation circuits and the package plane modeled by a transmission line matrix (TLM) method [6].

2 Quarter-Circle Shaped Plane Cavity Resonance

Fig. 1 shows a simple structure of plane resonators that has a parallel plane with shorted end and an inductive load at one end. At the short end the voltage is minimum and the current is maximum. In a transmission line a standing wave is formed by the superposition of two waves propagating in opposite directions. However, in the case of parallel plate there are lots of reflected wave from the edge of the plane. A standing wave has the same phase in the whole plane, however the amplitude is different with the position of the plane. The different amplitude of the wave which makes the signal skew is related to the length from the incident point of the signal. In the square plane resonator of Fig. 1(a) diagonal corner has a relative long distance from the incident point than the other corners. Quarter-circle shaped resonator can compensate the mismatch of the length as shown in Fig. 1(b).

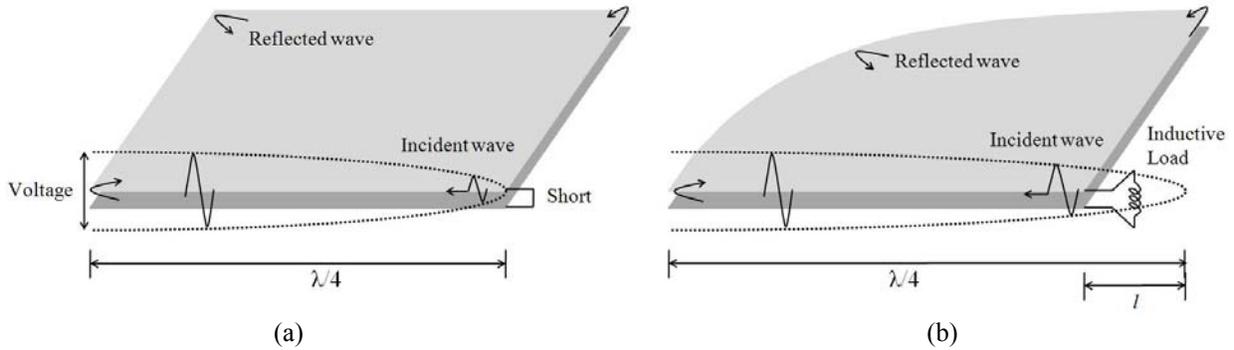


Fig. 1 (a) Square plane resonator (b) Quarter-circle shaped plane resonator with inductive load for frequency control

The external circuits can be used as the excitation of this resonator near shorted end and destination local buffers can be connected to the edge of open end. However, the resonant frequency just decided by the plane size is hard to change. To overcome these problems, an inductive load replaces the short end as shown in Fig. 1(b). An inductive load works as the extension of the plane, so the resonant frequency is decreased comparing with the open-short parallel plane.

3 Clock Distribution Network Using Plane resonator

Fig. 2 shows the proposed clock distribution network structure. The differential clock signals which are generated from voltage-controlled oscillator (VCO) and harmonic rejection mixer (HRM) are connected to the planes embedded in the package with bond wires in one corner, so these are input port of the plane. For single frequency resonant excitation HRM is used for output driver [7]. The output of the three differential amplifiers is summed to generate the final output signal. These sub-amplifiers are driven by the three phase-shifted square waves, for example, 0, 45 and 90 degree. A 4-stage ring VCO is adopted for octal phase generation for HRM inputs and the outputs of the VCO are converted to current mode swing in current mode pre-output drivers. A lumped inductor is modeled as inductive load near the input port, and 1nH inductance is used. Three points of the output port are simulated with this structure.

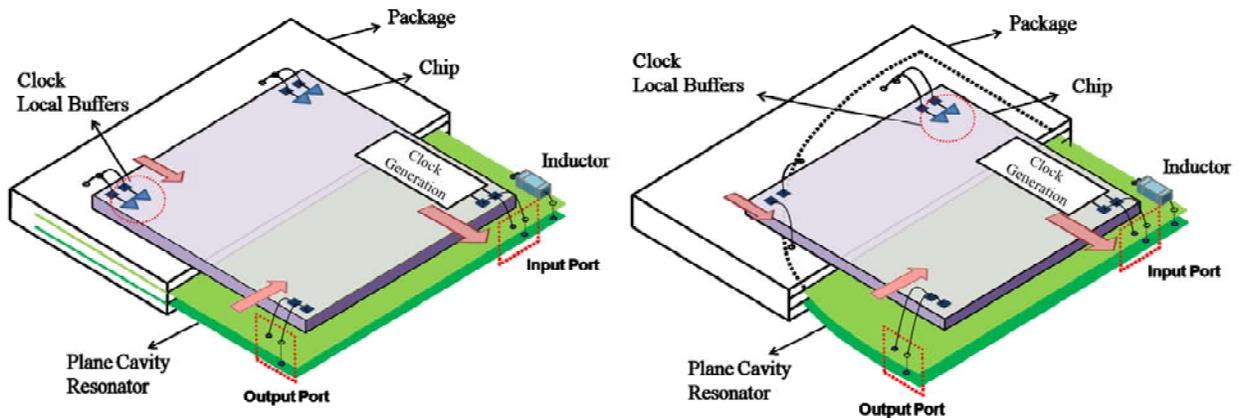


Fig. 2 Basic architecture of the proposed clock distribution network
(a) Square plane cavity (b) Quarter-Circle shaped plane cavity

Fig. 3 shows the whole model of the CDN using package plane resonance. On-chip circuits and the inductive load are located in the right-top corner of the plane. TLM model is used for plane cavity and bond wires are modeled as inductors and input capacitance of local buffers is also included. Square plane and quarter-circle plane cavity is compared in the view of skew.

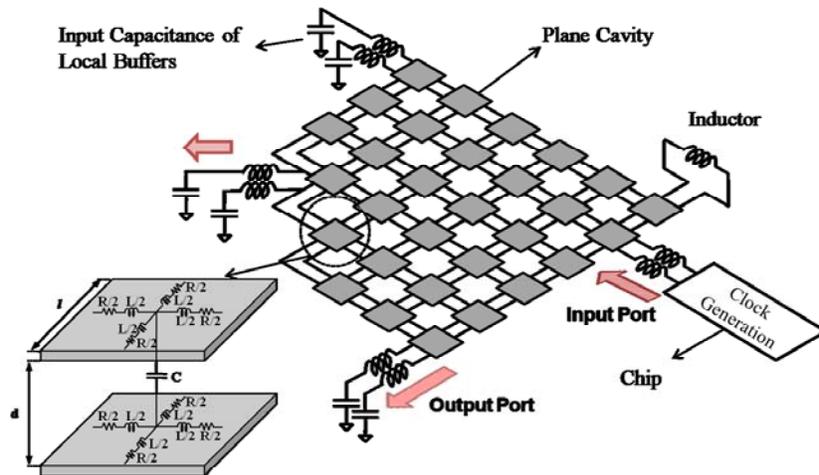


Fig. 3 Simulation model of the proposed scheme - Circuits, TLM model for planes and inductance for bonding wires

4 Verification of Reduced Jitter and Skew-free CDN

Jitter is simulated with power/ground noise. On-chip circuits of VCO and HRM can have SSN with digital logic and random noise is assumed for convenience. Fig. 4 shows the jitter of the input port and the one of the output ports. As the power/ground noise increases, pk-to-pk jitter of input port increases. Although the source has jitter over 20ps, distributed clock has jitter under 15ps. Time-domain differential clock signals at all output ports are compared in Fig. 5(a). The source clock is almost sinusoidal because of the HRM output driver. The target frequency of the clock source is controlled by VCO control voltage and resonant frequency of the plane resonator is controlled by the loaded inductance. The resonant frequency of the radius 10mm quarter-circle plane with 1nH inductance is 1.35 GHz. Time domain simulation is performed with clock cycle time 741ps. In the case of square plane resonator the skew of output ports is 3ps. The clock signal at the diagonal corner of the input port has a delay, which causes the skew. The length from the input port to diagonal output port is larger than the other ports. The additional length has additional phase delay and different standing wave amplitude. Quarter-circle plane resonator can reduce the mismatch of the length between input port and output ports. The skew is reduced to 0.5ps with quarter-circle plane resonator as shown in Fig. 5(b),(c).

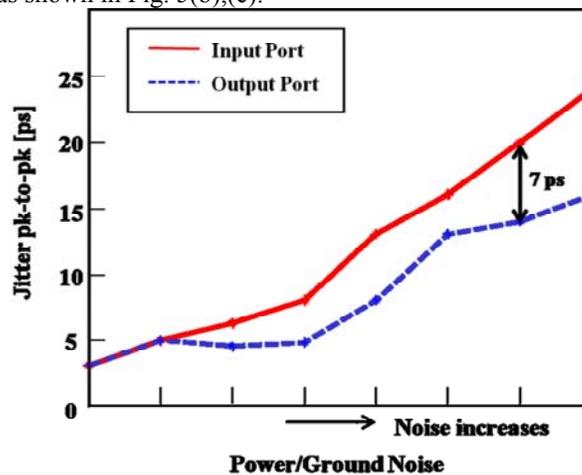


Fig. 4 Simulated jitter at the input and output ports with power/ground noise

5. Conclusion

We have described a CDN using plane cavity resonance. A CDN using square plane resonator can achieve low jitter and low skew clock distribution. Furthermore, skew-free clock distribution is possible with a quarter-circle plane resonator. The skew improvement due to a quarter-circle plane resonator was verified with chip-package

hybrid simulation. The jitter at the output port of the resonator is suppressed through a resonator, so clock is not only distributed and re-generated. The resonant frequency of the resonator is tunable with an inductive load. Low loss off-chip plane is used for clock distribution, therefore, the proposed clock scheme can significantly reduce the effect of on-chip power supply noise.

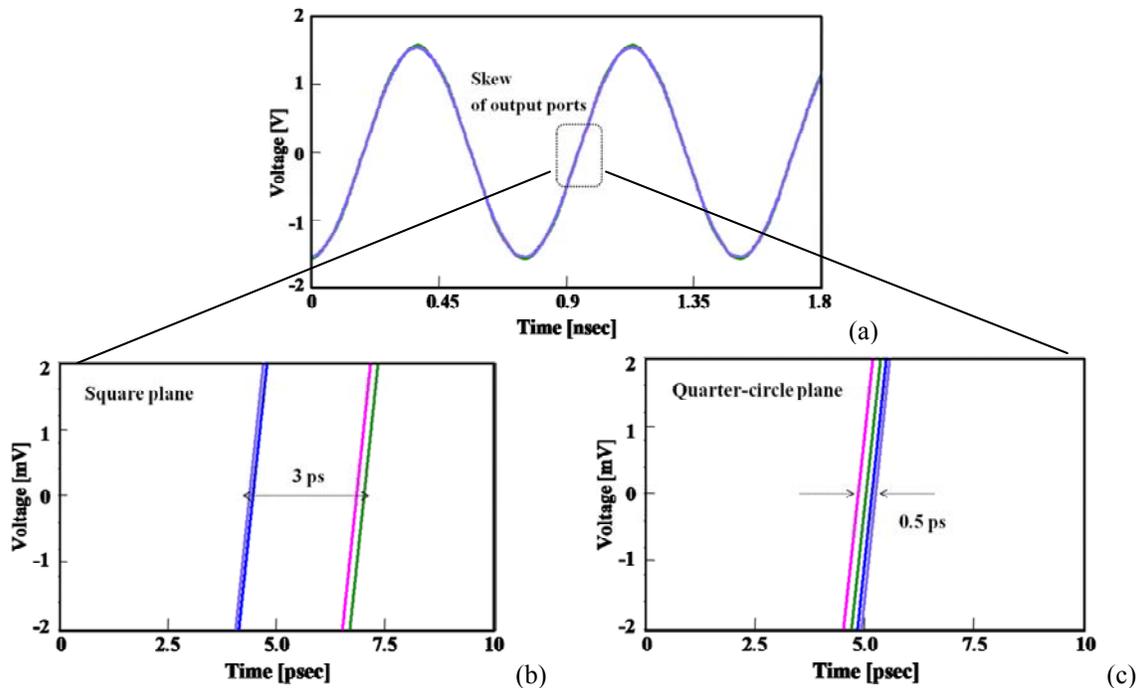


Fig. 5 (a) Simulated time-domain clock signal at the output ports
 (b) Skew of square plane resonator (c) Skew of quarter-circle shaped plane resonator

6. References

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