

Multi-Stacked Through-Silicon-Via Effects on Signal Integrity and Power Integrity for Application of 3-Dimensional Stacked-Chip-Package

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Abstract

We investigate the multi-stacked through-silicon-via (TSV) effects on signal integrity (SI) and power integrity (PI) depending on number of stacked TSVs. A single SG (Signal/Ground)-TSV-pair shows very small serial inductance (< 30 pH) due to its small height (80 μm), but very large serial resistance (70 m Ω) due to its small diameter (~ 80 μm) and shunt capacitance (> 4 pF) due to its thin SiO₂ (0.2 μm) between TSV and silicon substrate. In multi-stacked TSV case for high frequency application, SI becomes worse due to its resistance and capacitance, but PI becomes better due to its inductance and capacitance.

1. Introduction

System in Package (SiP) is the highest technology to make mobile electronic devices such as cell phones, personal digital assistants (PDAs), digital cameras, and etc, be small enough for men to carry them in one hand. Therefore, the demands for SiP are dramatically increasing and predicted from 1,573 million units in 2007 to 2,495 million units in 2011, and the most part of SiP applications in 2007 is concentrated in cell phone by 71 % [1].

However, the conventional SiP is manufactured with a few chips are located on a single package substrate and long wire-bonding. Consequently, though individual data processing speed of chip is high, the overall system performance is not enough to meet current demands due to the long wire-bonding interconnections. Therefore, 3-dimensional (3-D) stacked-chip-package is highly needed to get short signal and power supply path (PSP) for enhancing qualities of signal integrity (SI) and power integrity (PI) by shortening interconnection length between semiconductor chips. These packages are suitable for small and lightweight mobile electronic devices. Also, these devices need low power consumption package for increasing battery replacement or recharging cycle.

At the first trying for 3-D stacked-chip-package, a wire-bonding interconnection is adopted by Hynix, Samsung, and Akita Elpida. They stacked very thin chips (25 μm \sim 30 μm thickness/chip) in shape of stairs and connected the chips each other and the chips to package substrate. This method efficiently reduces wire-bonding length between chips and SiP size. Moreover, it increases chip density in a unit area. The high chip density is very important in case of memory chip stacking. The world wide market volume of 3-D stacked-chip-package is predicted from 2,065 million units in 2007 to 5,227 million units in 2011, which is almost double [1].

A conventional bonding-wire interconnection for the 3-D stacked-chip-package is not the best way to guarantee good signal integrity (SI) and power integrity (low power and noise) due to its large equivalent series inductance (ESL) and large conduction loss. Therefore, the technologies for reducing inter-chip interconnection length are developing. The state-of-the-art technology of them is through-silicon-via (TSV), which routes the electrical signal and PSP through all stacked chips, rather than wire-bonding. TSV is a promising interconnection method to connect vertically stacked chips with the shortest interconnection, which means the lowest ESL and conduction loss interconnection are provided to both signal and PSP between semiconductor chips. Therefore, in order to design advanced 3-D stacked-chip-package using TSV, the precisely evaluated SI and PI of single SG (signal/ground)-TSV-pair depending on number of stacked TSVs. However, since most parts of TSV manufacturing technology are under developing, it is very difficult to evaluate them through measurements. Consequently, 3-

dimensional (3-D) full wave electromagnetic (EM) solving method is adequate to investigate multi-stacked through-silicon-via effects on SI and PI for application of 3-dimensional stacked-chip-package.

2. Electrical Modeling of Through-Silicon-Via (TSV) for 3-Dimensional Full Wave Electromagnetic Solving

First of all, in order to investigate SI and PI of TSV depending on number of stacked TSV, we have evaluated electrical characteristics such as S-parameters of TSV-pair, one is for signal current path (S) and the other is for return current path or ground (G). Two TSVs used for this paper is called by single SG-TSV-pair. Then we have selected large size (80 μm) and large pitch (200 μm) TSVs for single SG-TSV-pair in a silicon (Si) substrate with 80 μm thickness, 10 $\Omega\text{-cm}$ resistivity, and 0.2 μm thickness silicon oxide (SiO_2) on its all surfaces based on the structures used in [2-5] (Fig. 1). SiO_2 is always used when TSV is formed in Si because Si is semiconductor and it is needed to block DC leakage from TSV to Si substrate. And we have constructed the 3-dimensional electrical model of single SG-TSV-pair as shown in Fig. 1, and extracted its S-parameter (Fig. 2), which has two-port results between top and bottom surfaces of single SG-TSV-pair from 100 MHz to 30 GHz. 30 GHz bandwidth can support 10 Gbps (Giga bit-per-second) digital signal data when considering 6th harmonics of digital signal data.

In order to easily understand of electrical characteristic of single SG-TSV-pair, we plot only S21 magnitude and phase on Fig. 2 from 100 MHz to 30 GHz with log scale. As shown in Fig. 2, single SG-TSV-pair has large capacitance (rapid slope from 100 MHz to 400 MHz) due to very thin (0.2 μm) SiO_2 between TSV and Si substrate, and makes non linear phase delay up to 1 GHz. Large resistance is shown due to small size TSV and large loss of Si substrate between two SG-TSVs.

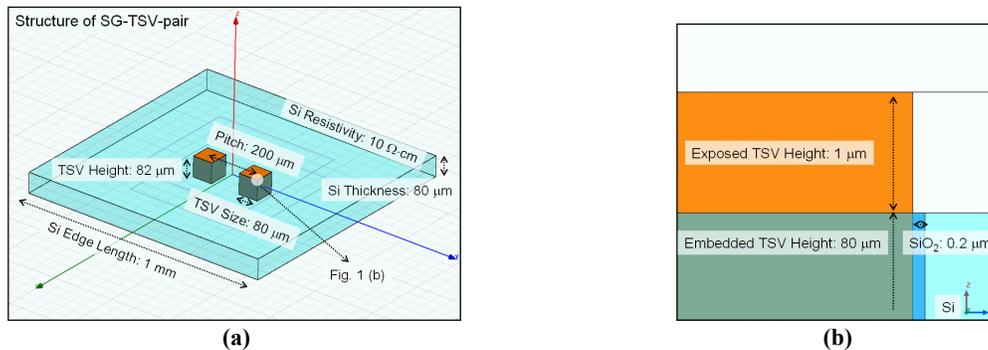


Figure 1. (a) 3-dimensional electrical model of single SG-TSV-pair (b) SiO_2 structure between TSV and Si substrate.

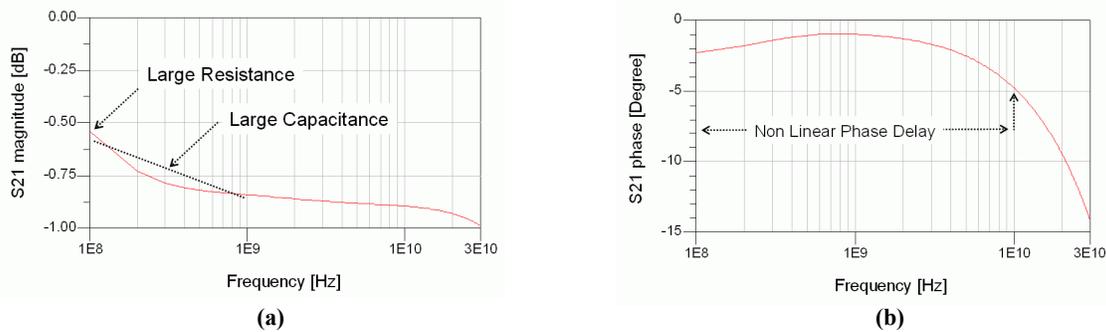


Figure 2. Extracted S21 magnitude (a) and S21 phase (b) of single SG-TSV-pair (Fig. 1) by using 3-D full wave EM solving method. (x-axis and y-axis have log scale)

3. Multi-Stacked Through-Silicon-Via (TSV) Effect on Signal Integrity (SI)

It is very difficult to obtain S-parameters of multi-stacked TSV even though 3-D full wave EM solving method is used. Therefore, we have obtained S-parameters of multi-stacked TSV by using S-parameter of single SG-TSV-pair and cascading them based on ABCD-parameter concept. For example, if we want to obtain S-parameter of 2-stacked TSV, we cascade two S-parameters of single SG-TSV-pair. Then, we obtained transmitted 10 Gbps digital

signal data through multi-stacked TSV by using Spice Type simulation tool. Figure 3 shows S-parameters of multi-stacked TSVs (a), and the transmitted 10 Gbps digital signal data (b-d) when blue line is for 2-stacked TSV, sky blue line is for 5-stacked TSV, and pink line is for 10-stacked TSV, respectively.

As number of stacked TSVs is increased, the total resistance and total capacitance are increased because a serial resistance and a shunt capacitance of each single SG-TSV-pair is connected each other in multi-stacked condition. These increased values make 10 Gbps digital signal data distorted from lossless signal shape (eye open: 0.5 Vp-p and 0.05 ns rising and falling times). When comparing Figs. 3 (b), (c), and (d), signal DC level decreases from 0.4 Vp-p to 0.2 Vp-p, and rising and falling times varies from 0.04 ns to 0.1 ns. Especially, Fig. 3 (d) shows very abnormal result because its rising and falling times are shorter than those of lossless signal shape. However, it can be explained by very large DC drops (0.2 Vp-p DC level), which makes the rising and falling times shorter.

As a result, in order to use multi-stacked TSV for high frequency application, the resistance and the capacitance of single SG-TSV-pair must be reduced by increasing Si substrate resistivity and reducing TSV size such as height and diameter, which reduce effective area of surface between TSV and Si substrate.

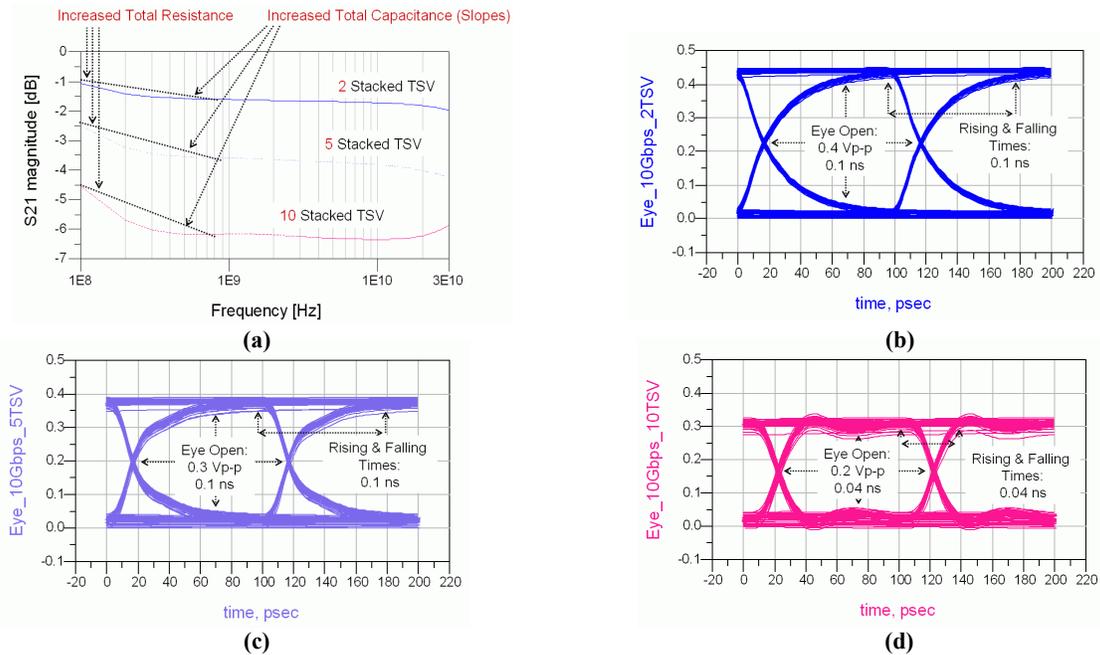


Figure 3. (a) S21 magnitudes of multi-stacked TSV. (b), (c), and (d) are the transmitted 10 Gbps digital signal data. Blue lines (a, b) are for 2-stacked TSV, sky blue lines (a, c) are for 5-stacked TSV, and pink lines (a, d) are for 10-stacked TSV.

4. Multi-Stacked Through-Silicon-Via (TSV) Effect on Power Integrity (PI)

The previous chapter 3 said that multi-stacked TSV effect on signal integrity for TSV application to signal path, and TSV structure and material has to be optimized to be applied to high frequency inter-chip data link. And there is another inter-chip link such as PSPs. Since electrical performance of inter-chip PSP is limited by ESL, which increases input on-chip PSP impedance, of inter-chip PSP and package substrate for multi-stacked TSV, the low ESL and large capacitance of multi-stacked TSV are very helpful. In this chapter, we consider and compare two cases as shown in Fig. 4. Fig. 4 shows 3 parts for 3-D full wave EM solving such as TSV (a), wire-bonding ($\phi = 25 \mu\text{m}$) (b), and package substrate ($20 \text{ mm} \times 20 \text{ mm} \times 0.2 \text{ mm}$). Fig. 5 (a) shows the input PSP impedance of package substrate without any inter-chip interconnections, and its large capacitance (75 pF) and ESL (1.69 nH) before and after self resonance frequency (430 MHz) respectively. And we have connected on-package PSP and inter-chip PSPs as shown in Fig. 4, and obtained input on-chip PSP impedances depending on number of stacked TSVs as shown in Fig. 5 (b). When wire-bonding is added as an inter-chip PSP on 10 stacked chips, the input on-chip PSP impedance increases due to large ESL of wire-bonding up to 2.6 nH (red line of Fig. 5 (b)). Even 2 stacked chips with wire-bonding shows 2.3 nH ESL. While, TSV applied inter-chip PSP on 10 stacked TSV shows low input on-chip PSP impedance through all frequency range due to large capacitance and low ESL of TSV and shows 360 pF

capacitance and 1.8 nH ESL (blue line of Fig. 5 (b)). Sky blue and pink lines of Fig. 5 (b) are the input on-chip PSP impedances of 2 and 5 stacked TSVs respectively. As a result, we can know that the larger dimensions such as diameter and height and the smaller pitch of SG-TSV-pair give the lower input on-chip PSP impedances to the input on-chip PSP, and consequently induce lower noise on power supply system in case of multi-stacked TSV.

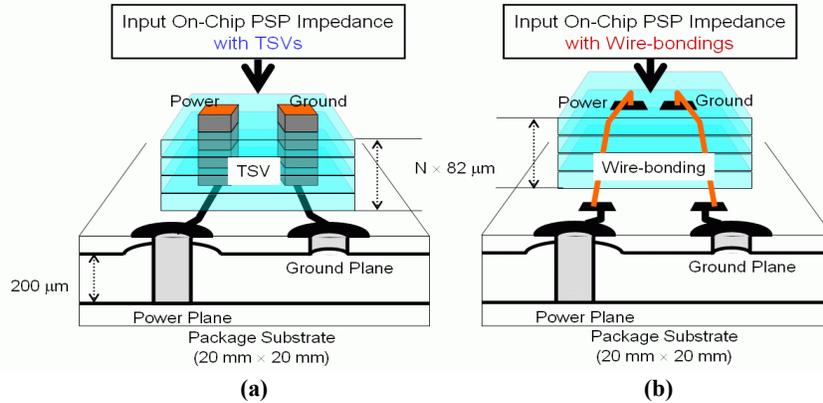


Figure 4. Electrical models for comparison of input on-chip PSP impedances depending on inter-chip interconnection types such as multi-stacked TSV (a) and wire-bonding (b). N is the number of stacked chips.

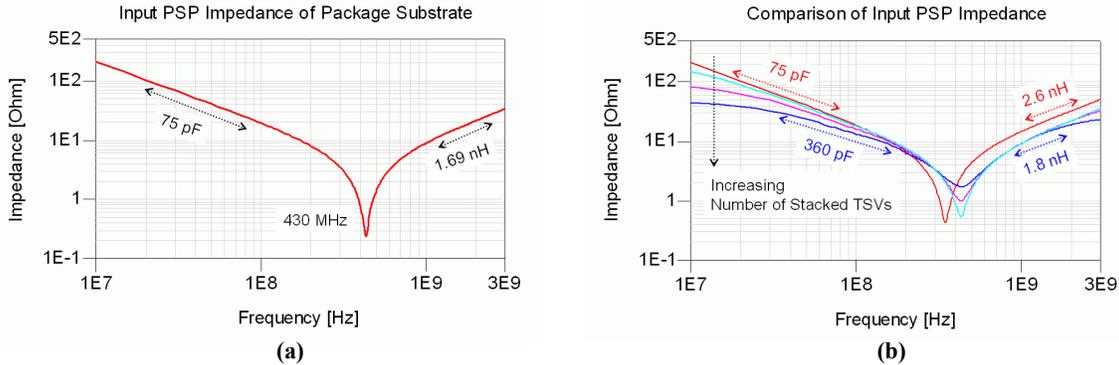


Figure 5. (a) Input PSP impedance of package substrate. (b) Input on-chip PSP impedances of Fig. 4 (a) and (b) when 10 stacked chips with wire-bonding (red line), 10 stacked TSV (blue line), 5 stacked TSV (pink line), and 2 stacked TSV (sky blue line) are connected to PSP of package substrate.

5. Conclusion

In this paper, we have investigated multi-stacked TSV effects on SI and PI of 3-D Stacked-Chip-Package. To enhance the SI of multi-stacked TSV, we have to select smaller size TSV with larger resistive Si for smaller capacitance and resistance. While, we have to select larger size TSV to get larger capacitance and lower input on-chip PSP impedance when multi-stacked TSV is connected to PSP of package substrate.

6. References

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