New Generation Correlators

John D. Bunton
CSIRO ICT Centre
PO Box 76, Epping, 1710, Australia
email: john.bunton@csiro.au

INTRODUCTION

In the past five years considerable progress has been made on new cost-effective designs of large correlators. The same techniques also provide efficient beamformer architectures. The resulting designs are not only applicable to radio astronomy, where they are being trialled, but also in communications and imaging systems. The use of beamformers in communications and imaging are commonplace, and correlators can be used for fast acquisition of W-CDMA signals.

FX CORRELATORS

Correlators can measure the cross correlation function which can then be Fourier Transformed to produce the cross power spectrum (XF correlator) or they can measure the cross power spectrum directly (FX correlator). The architecture of these two approaches is shown in Figure 1.

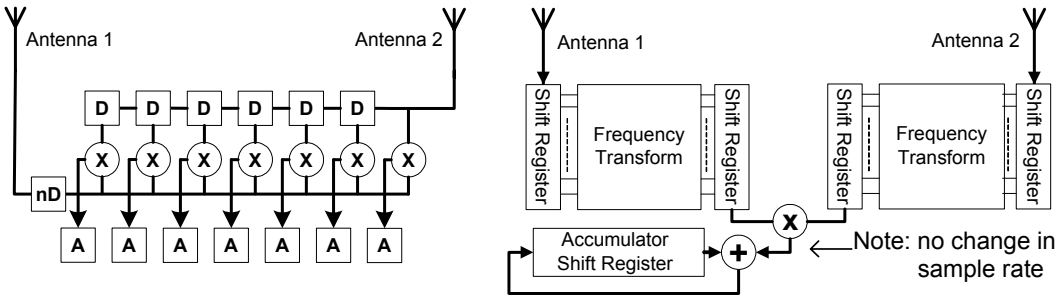

Figure 1 Architecture of an XF (left) and FX (right) correlator

In the XF correlator the number of complex multipliers per baseline is equal to the number of frequency channels N, for simplicity it is assumed the multiplier and the data clock are at the same rate. In the FX correlator only one multiplier per baseline is needed for the cross multiply. However there are the additional multipliers in the frequency transform. Each frequency transform needs $10k$ complex multiplies, where k is an implementation dependent term that is approximately one. In a system with M inputs there are M frequency transforms and $M(M-1)/2$ baselines so on average the frequency transforms add $20k/(M-1)$ multipliers per baseline.

Thus the FX correlator has fewer multipliers whenever $N > 1 + 20k/(M-1)$.

For example, for the Australia Telescope with 6 antennas the break even point is less than ten frequency channels. In the SKA [www.skatelescope.org] the specifications call for 10,000 frequency channels and hundreds if not thousands of antennas. In this case the FX design has orders of magnitude fewer multipliers, greatly reducing cost and power consumption.

CORRELATOR EFFICIENCY

In recent times most correlators built have been XF correlators partly because of the NRE cost of designing a frequency transform engine and other factors. With the arrival of cost effective Field Programmable Gate Arrays (FPGAs) this ceases to be a major factor. The design is now implemented in Hardware Descriptor Language such as VHDL or Verilog and errors can be corrected in hours instead of months as was the case with dedicated Application Specific ICs. This allows the designs to be easily migrated to other system.

The FX correlator has also suffered from reduced correlator efficiency because the traditional approach involves taking the FFT of non-overlapping data blocks [1,2]. This leads to a 1.22 times increase in correlator noise for narrow band signals [3], equivalent to a correlator efficiency of 0.82.

This loss is due to the block nature of the processing leading to higher delay lag values being undersampled as well as the time aliasing resulting from the circular convolution being used.

In Figure 2 it is seen that with block processing, the signal to noise performance is poor for high lag values. A solution to this problem is to average adjacent frequency channels [3]. In the lag domain this has the effect of windowing the cross correlation function, which suppresses the high lag components. For the same frequency resolution, a larger FFT is needed but this does not significantly increase the compute load, only the memory requirements. This approach is being used in the correlator being built for the ALMA Compact Array [4].

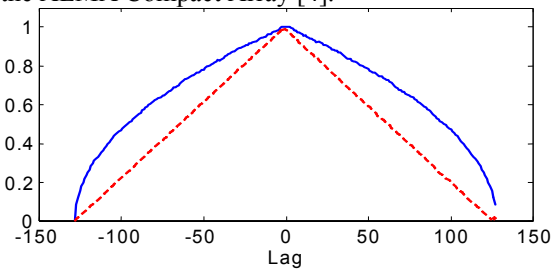

Figure 2 Average power for the block-processing cross correlation of independent white noise (solid line), and identical noise inputs (dotted line).

An alternative method of improving correlator efficiency is to overlap the data blocks [2]. This has the problem that the processing cost goes up in direct proportion to the degree of overlap, making this approach unpopular. A more efficient approach is the polyphase filterbank [5, 6, 7], which is being implemented on the Alan Telescope Array (ATA) [8], Australia Telescope [7], DSN Array-based Network[9], and SKAMP [10]. The latter will be in common with the proposed CSIRO xNTD and MIT Mileura Wide Field Array and the same design is being adapted for a mm-wave beamformer at CSIRO. The polyphase filterbank is a decimated form of overlapped block processing where each block is multiplied by a time window [11]. For a time window such as the one shown in Figure 3 the frequency channels are close to ideal but many are redundant.

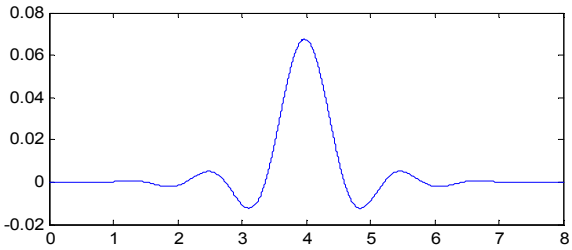

Figure 3 Time window for 8 times overlap system, (block advance is 1/8 of block length)

Removing the redundant channels is equivalent to decimating the output of the FFT. With a suitable choice of time window and decimation factor the output data rate is the same as that for a non-overlapping block FFT correlator. However, the multiply load for the frequency transform is high. This is brought down by eliminating redundant calculation and the resulting structure is a polyphase filterbank, Figure 4. With eight point pre-filters $p_i(m)$ the added noise due to block processing reduces the correlator efficiency to 97.5. A 10% time oversampling at the output of the filterbanks increases the correlator efficiency to 99.5.

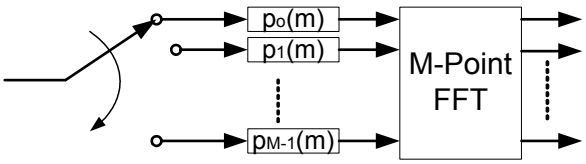

Figure 4 Analysis Polyphase filterbank

Another source of efficiency loss in correlators is due to the coarse digitisation that is used. When hardware costs dominated, 1 and 2-bit digitisation was used, leading to a correlator efficiency due to quantisation of 0.64 to 0.88. In the new correlator for the Australia Telescope (AT) [7] a full 8-bit data path is used leading to negligible correlator loss. The ALMA Compact Array is using 3-bit data, and many other designs are using 4-bit data which gives a correlator efficiency of 0.99. Total correlator

efficiency is the product of the correlator efficiencies due to quantisation, block processing and analogue to digital quantisation. For new designs, the last term can be neglected as converters with 8 or more bits of precision are now used.

MEMORY REQUIREMENTS

Use of an FX correlator minimises the multiplier requirements but not the memory. For the SKA there are ~10,000 frequency channels, up 10,000 antennas and 6 bytes per correlation. For full Stokes parameters up to 1.2 Tbytes of memory is needed on the correlator chips. With current FPGAs having less than 1 Mbyte of memory it is better to use external DRAM for storage with on-chip storage for the single frequency channel currently being processed [12]. This creates an I/O bottleneck into the DRAM which is solved by buffering the input data. Assuming all baselines for a single frequency channel can be processed at one time then a long time series of data for that channel can be processed before the data must be accumulated in DRAM. This technique can reduce the data rate into DRAM by a factor of 1000 or more and the on-chip memory requirements are reduced by a factor of 10000.

DATA FLOW

If each cross multiply unit processes the full bandwidth, as is often done, then each correlation module can process a small fraction of the baselines in an SKA correlator. To process all the baselines the same antenna data must be sent to multiple correlation modules greatly exacerbating the problem of routing data within the correlator. In an FX correlator the solution is to process a fraction of the total bandwidth in each correlation module [13]. This is achieved by putting a cross-connect between the filterbanks and the correlation modules. A simple example of this cross connection is shown in Figure 5. Much of the cross connection can be done on the backplanes of the filterbank and correlation modules. For the SKA possibly one extra layer of cross connection is sufficient and the total cost of routing the data is just twice that of minimum possible.

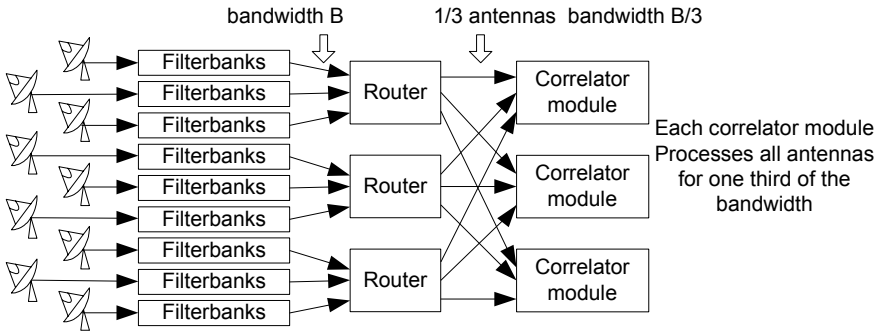

Figure 5 Cross connections for nine groups of antennas into three correlator modules

A fibre optic solution could make the cross connect cost negligible. In this approach the filterbanks are at the antenna. Data for groups of antennas are sent to the correlator using dense wavelength division multiplexing. A fixed optical router then sends the appropriate wavelength to the appropriate correlator module. Each wavelength carries a fraction of the bandwidth for all antennas in the group.

The architecture in Figure 5 also provides an efficient implementation of broadband beamformers [9]. As with a correlator, data from all antennas must be aggregated together and the above architecture decimates the bandwidth so single modules can do this. If needed, the time series for the beam can be generated by using a synthesis polyphase filter bank which uses the same building blocks as the analysis filterbank shown in Figure 4 with the order of operation reversed.

Another area which can have problems is data flow into the packaged correlator integrated circuits ICs either custom integrated circuits or FPGAs. Internally the multipliers in correlation ICs have been arranged as a systolic array. The number of inputs needed is equal to twice the square root of the number of multipliers. As the capabilities of correlator ICs increase the data input into the IC becomes the bottleneck. One existing design [14] proposed an IC with I/O capabilities exceeding 0.5Tbits/s. I/O into the chip is reduced by the use of local storage. One approach [8] loops the data through a shift register and at each register the input data and delay input data is available. At each register output M correlation are formed that must be stored in M accumulators. In this design the I/O is independent of

the number of antennas. An alternative approach includes antenna data storage with each multiplier. For example with storage for two sets of 16 antennas 256 correlations are formed and the data rate to the multiplier is reduced by a factor of 16. For the high speed correlator chip proposed in [14] the input data rate is reduced from 6 Gbit/s to 0.375 Gbit/s. In any design there will be a trade-off between on-chip memory and input and output data rates with the optimum solution changing as technology advances.

CONCLUSION

FX correlators have a lower computational cost than XF correlators in next generation correlators. The same FX architecture can be use to implement beamformers. Problems associated with low correlator efficiency have been addressed by channel averaging or the use of polyphase filterbanks. Use of polyphase filterbanks also allows reconstruction of the time series in beamformer application. I/O bottlenecks can occur between the filterbanks and cross multipliers or beamformers, but a solution is a cross connect that allows each correlation module to fully process a small part of the bandwidth. High on-chip memory requirements are eliminated by reordering the data. In the correlation ICs some additional memory reduces input data rates. Taken together these advances make high performance correlators and beamformers viable. In particular, there is confidence that the SKA correlator and beamformer can be built.

ACKNOWLEDGEMENTS

These advances have resulted from simultaneous efforts at Nobeyama, Berkeley and Sydney. In particular the author would like to recognise the work of Yoshiro Chikada, Lynn Urry and Dick Ferris. The author also wishes to thank Colin Jacka for his input into this paper.

BIBLIOGRAPHY

[1] Chikada Y., et al.:1984 'Digital FFT Spectro-Correlator for Radio astronomy', in Indirect Imaging (ed J.A. Roberts), Cambridge University Press, pp387-404, 1984
[2] Chikada, Y, et al.:1987 'A 6 x 320-Mhz 1024-Channel FFT Cross-spectrum Analyzer for Radio Astronomy,' Proc IEEE 75, 9, pp 1023-1209, September 1987
[3] Okamura, S.K., Chikada, Y., Momose, M., Iguchi, S.:2001 "Feasibility Study of the Enhanced Correlator for 3-way ALMA I.", ALMA memo 350, February 2001, http://www.nrao.alma.edu/memos/
[4] Tsutsumi,T., Morita, K., Hasegawa, T., Jerome Pety, J.:2004 'Wide-Field Imaging of ALMA with the Atacama Compact Array: Imaging Simulations' ALMA memo 488 http://www.alma.nrao.edu/memos/
[5] Bunton, J.D:2000 'An Improved FX correlator', Alma Memo 342, Nov. 2000 http://www.alma.nrao.edu/memos/
[6] Bunton, J.D.: 2005 'SKA Correlator Advances' Experimental Astronomy (In press)
[7] Ferris, R.H., Bunton, J.D., Stuber, B.:2001 "A 2GHz Digital Filterbank Correlator", The SKA: Defining the Future, Berkeley California, July 9-12, 2001. http://www.skatelescope.org/skaberkeley/html/posters/pdf.htm
[8] Urry, W.L., 2002, 'The ATA Imager', ATA memo 39, Jan 2002 http://astron.berkeley.edu/ral/ATAMemo39.pdf
[9] Bunton, J.D. & Navarro, R.:2005 'DSN Deep-Space Array-based Network Beamformer', Experimental Astronomy in press
[10] Warr, G.B. et al., 'Prototyping SKA Technologies at the Molonglo Radio Telescope', WARS02, Leura, Australia, 20-22 February 2002 paper J8 http://www.ips.gov.au/IPSHosted/NCRS/wars/wars2002/proceedings/comm-j/screen/warr.pdf
[11] Bunton, J.D.:2003 'Multi-resolution FX Correlator', ALMA memo 447, Feb 2003, http://www.alma.nrao.edu/memos/
[12] Bunton, J.D.:2001 'A Cross Multiply Accumulate Unit for FX Correlators', Alma Memo 392, Sep. 2001 http://www.alma.nrao.edu/memos/
[13] Urry, W.L.:2000 'A Corner Turner Architecture', ATA Memo 14, November 2000, http://astron.berkeley.edu/ral/ATAMemo14.pdf
[14] D'addario, L. & Timoc, C.: 2002 'Digital Signal Processing for the SKA', International SKA Conference 2002, Groningen, The Netherlands, 13-15 August 2002, http://www.lofar.org/ska2002/pdfs/D'Addario-correlator.pdf