DATA TRANSMISSION AND SIGNAL PROCESSING

FOR THE EXPANDED VERY LARGE ARRAY (EVLA)

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ABSTRACT

The EVLA Project will increase the bandwidth of the VLA by a factor of 80 compared to the original instrument. Each of the eight 2 GHz bandwidth IF signals are digitized at the antenna using a custom 4 Gsample/s, 3 bit/sample digitizer developed for the ALMA Project. For low frequency bands where RFI is heavy, each of four 1 GHz bandwidth IF signals are digitized using an Atmel 2 Gsample/s 8-bit digitizer. The total data rate from each antenna is 96 Gbit/s, and data is transported to the central correlator by a WDM digital fiber-optic system at distances up to 22 km. Data for two 2 GHz IFs enter the correlator in de-multiplexed form and, after geometric delay correction to +/-0.5 samples at 4 Gsample/s, are filtered with a bank of multi-stage digital filters into sub-bands. These sub-bands are individually correlated with custom 130 nm 2048 complex-lag, 4-bit correlator chips. The correlator can produce 16,384 spectral channels per baseline in wideband modes, and at narrower bandwidths up to 4 million channels per baseline using recirculation, all with a 60 dB spectral dynamic range. The correlator can integrate and bin into 2000 bins synchronous with a pulsar. Correlation products are accumulated in an off-chip long-term accumulator and transported via 1 Gbit/s Ethernet to backend computers for FFT, further integration, and interference mitigation. The correlator provides powerful and flexible signal processing capabilities making it suitable for the EVLA and potentially a wide variety of radio telescope configurations.

INTRODUCTION

The EVLA project aims to upgrade the VLA from its current 200 MHz of bandwidth to 16 GHz, and provide contiguous frequency coverage from 1 to 50 GHz. The antennas are being outfitted with all new receivers, the current waveguide transmission system has been replaced with a digital fiber optic system, and the correlator is being replaced with a new temporal and frequency-agile wideband, high spectral resolution, high spectral dynamic range correlator. Correlator hardware is modular and the EVLA correlator as well as other correlator configurations for both connected-element and non-real-time VLBI can be built for virtually any radio telescope's single-dish, array, and baseband configuration. The use of mezzanine cards and in-system programmable FPGAs (except for the custom correlator chip), as well as dual VSI-H I/O interfaces on each station board provide the correlator with a high degree of flexibility. This paper will describe the EVLA data acquisition, transmission, and correlation system and provide some insight into correlator flexibilities that could make hardware useful for other radio telescope installations.

DATA ACQUISITION AND TRANSMISSION

A simplified block diagram of the EVLA data acquisition system is shown in Fig. 1. There are four paths from the IF downconverters, and each path includes two 3-bit, 4 Gsample/s samplers, and a single 8-bit, 2 Gsample/s sampler with quasi-baseband inputs of 2-4 GHz and 1-2 GHz respectively.

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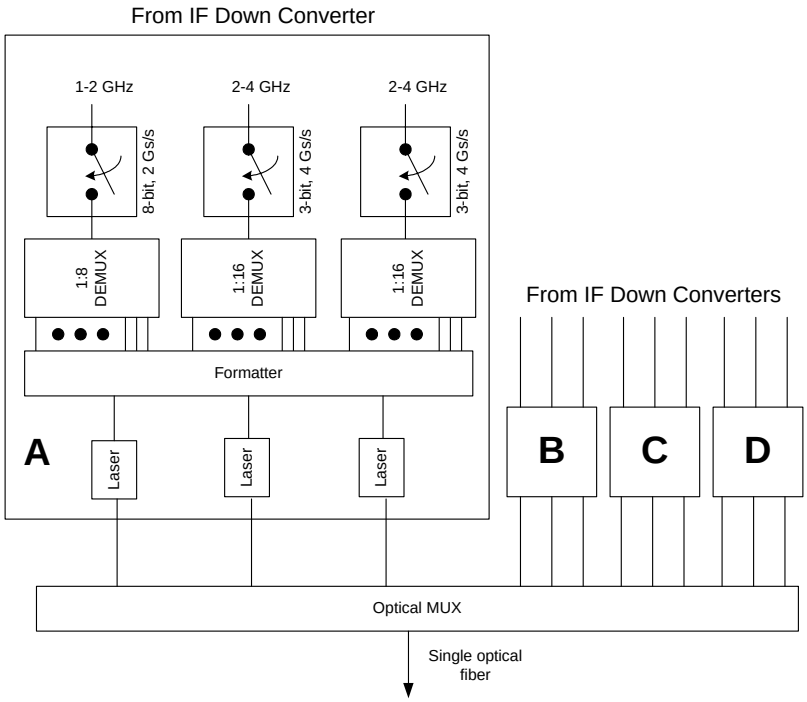

Fig. 1 Simplified EVLA antenna data acquisition block diagram.

All of the formatted digitized signals from all of the four IF down converters (A-D) are multiplexed onto a single fiber. Each of the 1550 nm WDM channels consists of a transmitter section of a Fujitsu 10 Gbit/s transponder. There are 12 fibers, including spares, in each buried fiber cable from each antenna pad to the central building. At the receiving end in the central building, the WDM channels are separated and three fibers enter the de-formatter mezzanine card mounted on each of the correlator's station boards. Here, the 10 Gbit/s formatted streams are de-multiplexed with an Altera FPGA using a 1:16 de-multiplexer made for SONET OC192 communications systems. The interface between the de-formatter mezzanine card and the correlator station board is three, 32-bit streams, each one operating at 256 Mbit/s. However, the interface definition includes an additional 32 bits for possible future expansion to 4-bit sampling.

CORRELATOR STATION-BASED PROCESSING

The correlator station board processes an IF pair consisting of two 2 GHz 3-bit sampled basebands or one 1 GHz 8-bit sampled baseband. Four station boards are required to process each EVLA antenna. The station board processes two 64-bit data highways—16x4 bits wide each. For the EVLA, only 3 bits of each 4-bit path is used for 3-bit sampling, and only one data highway is used for 8-bit sampling. Each of the data highways includes a 0.25 second geometric delay buffer for delay compensation correction to +/-0.5 samples at 4 Gsample/s on the 1:16 de-multiplexed data. This delay buffer is implemented on a mezzanine card and contains a controlling FPGA and SDR SDRAMs. After geometric delay compensation, each data highway enters a filter bank with 18 digital filter chips implemented in Xilinx Virtex-IV FPGAs.

Each filter chip produces one sub-band out of the wideband input with width programmable from 31.25 kHz to 128 MHz by using 1 or more of the filter's 4 stages. Placement of sub-bands in the wideband has some restrictions because of the poly-phase FIR/decimation step in stage 1, but each filter chip can otherwise have a different sub-band bandwidth and placement in the wide band. A simplified block diagram of the filter chip is shown in Fig. 2. The filter chip is the heart of station board processing and contains a number of features. An 8k-deep delay buffer can be used for "sub-band multi-beaming" so that the sub-band interferometer delay center can be offset from the wideband delay center by a small amount to permit wide-field imaging and in-beam phase referencing. Stage 1 is a 512-tap (256 taps in 8-bit input mode) poly-phase FIR filter. Stage 2 is a 64-512 tap filter complete with a high dynamic range DSSB mixer. Stages 3 and 4 are the same, but without the DSSB mixer. Sixteen bits are carried from one stage to the next so that there is only one re-quantization step to 4 or 7 bits before transporting the data downstream for correlation. The number of taps and decimation factors in stages 2-4 are such that a constant relative transition-band steepness is maintained independent of bandwidth, even down to the narrowest 31.25 kHz bandwidth out of stage 4.

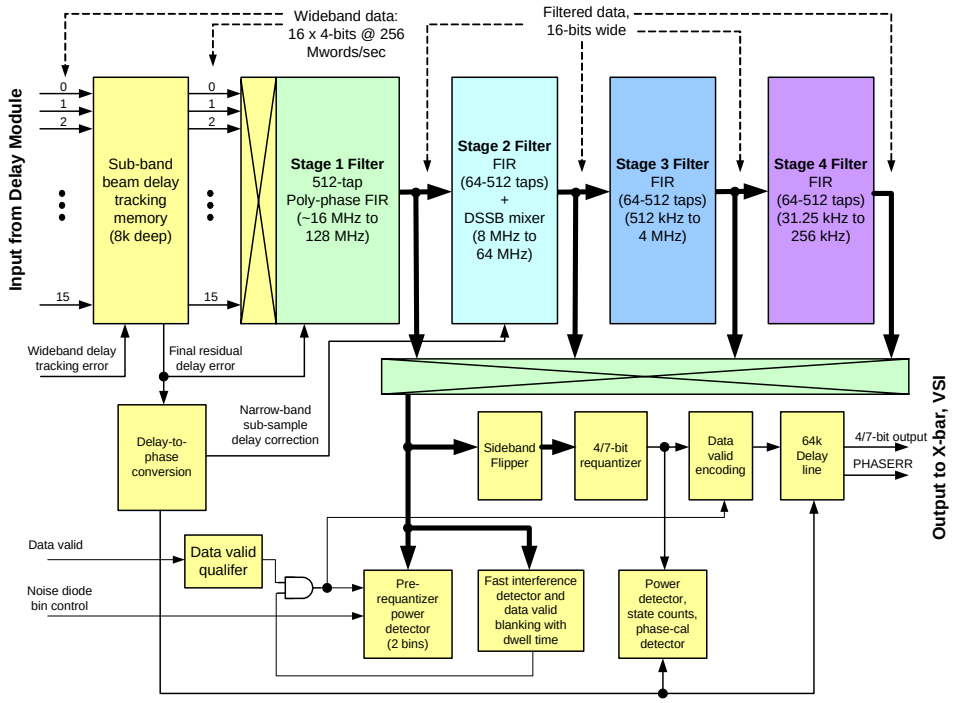

Fig. 2 Simplified block diagram of the filter chip.

The DSSB mixer in stage 2 can be used for finer placement of stage 2 sub-bands than afforded in stage 1. After filtering, a selection switch directs the 16-bit output to a side-band flipper and a re-quantizer with 4 or 7-bit re-quantization capability. Power before re-quantization is measured in one of two bins, synchronous with noise diode switching in the antenna for T_{sys} calibration. There is a fast interference detector/blanker with programmable thresholds and dwell times for blanking of burst interference. A post re-quantization power detector, state counter, and phase-cal detector are also provided.

After digital filtering into up to 18 sub-bands, the sub-band data (along with a real-time residual phase error for sub-sample delay correction for that sub-band) enter a cross-bar switch where they are directed to any of the 18 outputs on an output connector for transmission at a multiplexed data rate of 1.024 Gbit/s to downstream cross-correlators (Fig. 3). Distribution of the same sub-band data to multiple destination cross-correlators is required in some cases when correlator lags are split across cross-correlators. The station board also contains circuitry for transporting the 32-bit point-slope phase models and a high-speed station-based dump control signal to the cross-correlators for further processing.

CORRELATOR BASELINE-BASED PROCESSING

1.024 Gbit/sec multiplexed data streams enter the correlator baseline board where they are de-multiplexed and locked, aligned, and cross-bar switched before being fed to a row or column of 2048 complex-lag correlator chips arranged in an 8x8 array. The Altera Stratix-II chip that does the de-multiplexing, locking, and alignment, also contains logic and an external 512kx18 (x36 is an option) DPSRAM to perform recirculation functions, under command of the station-board generated high-speed dump control signal travelling with the data. Each of the eight correlator chips in a row or column receive the same data, and each one performs up to 16 cross-correlations in the 2048 complex-lag correlator chip. The correlator chip contains additional data path routing so that the sixteen sets of 128 complex-lag correlators can be arranged in a number of ways, depending on desired spectral resolution and bandwidth. The LO in each antenna is offset by a small epsilon frequency shift [1]; this shift, as well as earth-rotation phase, and the sub-sample delay error phase is removed using the correlator chip's *lag-based* 3-level phase rotator [2]. This method causes sub-band transition band aliasing as well as spurious interference and biases introduced after the LO shift to wash out rapidly with integration time, and depending on the magnitude of the frequency shift. Also, no earth-rotation phase correction or sub-sample delay interpolation by modulating the sampler clock phase at the antenna is needed—drastically simplifying the entire system.

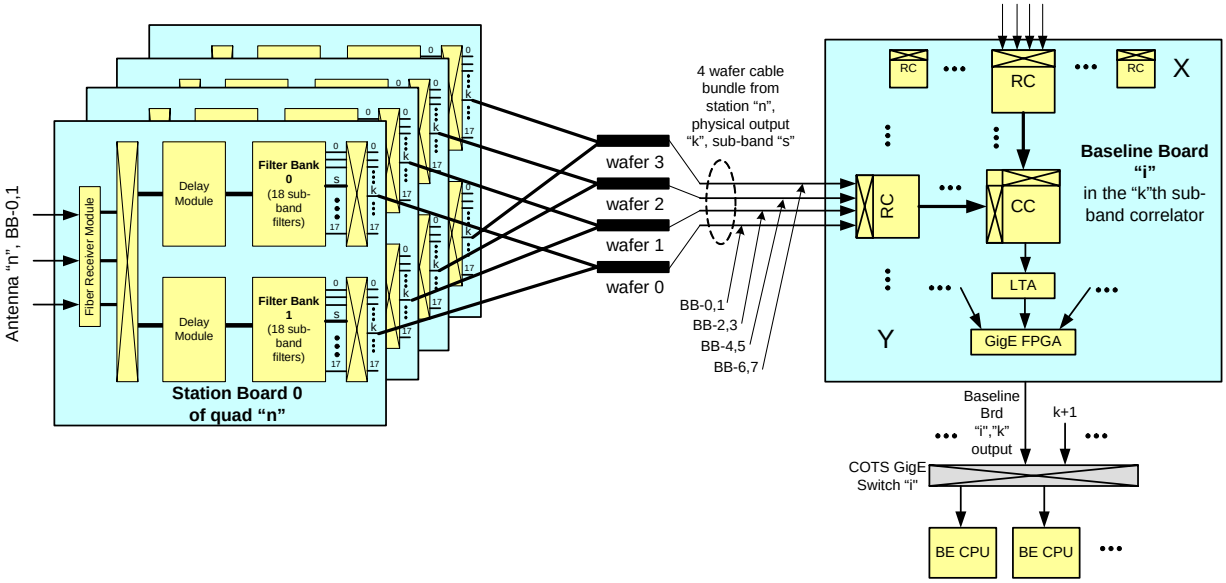

Fig. 3 Simplified EVLA correlator data routing.

After correlation, the coefficients are read out of the correlator chip, independent of a controlling CPU, and integrated in the long term accumulator (LTA). For performance, each correlator chip has its own LTA implemented in a small Altera Cyclone FPGA and external 16Mx16 DDR SDRAM chip, sized for 2000 pulsar phase bins for each correlation product. After long-term accumulation, integrated lag data are transported on 1 Gbit/s Ethernet via a GigE transmitter FPGA to the backend (BE) computers through a switched network for final processing—FFTs, integration, and interference excision. The final aggregate sustained output data rate from the backend is 25 Mbytes/s.

CORRELATOR FLEXIBILITIES

The correlator contains a number of flexibilities that could make it useful in other radio telescopes. Already, EVLA correlator hardware will be used in the e-MERLIN project. These flexibilities are as follows:

- The fiber receiver and de-formatter functions are on a mezzanine card—a different mezzanine card could be used if a different fiber interface is required..
- The 0.25 sec delay buffer is on a mezzanine card—different baseband channelization could be supported.
- Dual VSI-H interfaces; the station board can be used as a filter bank with VSI output or process VSI data.
- Stage 1 of the digital filter is able to perform sub-sample delay correction on multiple narrow baseband inputs.
- The cabling of the correlator is flexible and supports other configurations (e.g. such as for e-MERLIN).
- Increase bandwidth by adding station boards; increase spectral resolution by adding baseline boards.
- Data path switching and the correlator chip design permit each correlator chip to process up to 16 baselines.
- The correlator chip has an auto-correlator mode; each baseline board can perform 64 independent 2048 channel auto-correlations on 64 different bands, up to 128 MHz each.

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