Modeling and Analysis of Graded Channel Fully Depleted Cylindrical/Surrounding Gate SOI MOSFETs

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ABSTRACT

An analytical model for graded channel (GC) fully depleted cylindrical/surrounding gate SOI MOSFET has been developed to study the short channel effects (SCEs). The model assumes a steep transition for silicon film doping at the boundary of high/low doped regions and takes into account the effect of the doping and length of the two regions. The model is used to obtain the expressions of surface potential and electric field in the two regions. The analysis is extended to obtain an expression for threshold voltage (V_{th})

INTRODUCTION

Lateral channel engineering with graded channel doping has been investigated in order to address the problem of SCEs and hot carrier degradation in deep sub-micrometer regime [1-2]. In the present work, the impact of asymmetric channel profile is studied on a cylindrical/surrounding gate MOSFET [6]. An analytical model has been developed by solving the Poisson's equation in cylindrical coordinates. The variation of surface potential along the channel indicates that DIBL effect is considerably reduced. It is also found that V_{th} roll-off can be significantly reduced using a graded doping profile.

MODEL FORMULATION

Fig.1. shows a GC cylindrical gate MOSFET. The doping in the channel is kept high in a region of length L_1 near the source and low in a region L_2 near the drain such that the total channel length, $L=L_1+L_2$.
Therefore, the Poisson's equation in cylindrical coordinates in the two regions is:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\phi_i(r,z)\right)+\frac{\partial^2}{\partial r^2}\phi_i(r,z)=\frac{qN_{ai}}{\varepsilon_{si}} \tag{1}$$

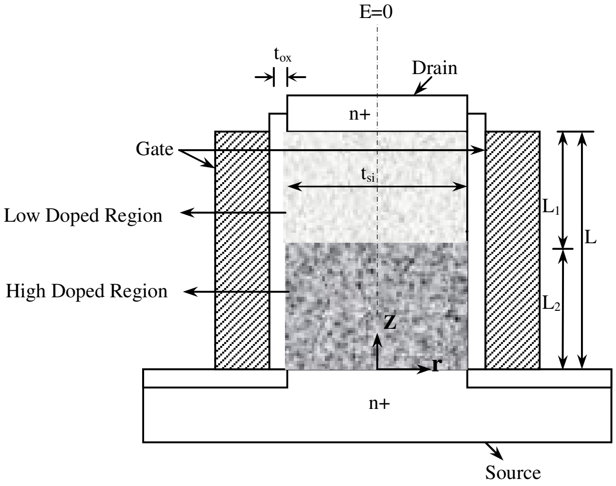

Fig.1 Schematic diagram of a GC FD CGT/SGT SOI MOSFET

where, $\phi_i(r,z)$, N_{ai} are the potential distribution in the silicon film and the doping in high/low doped regions (i=h for high doped, HD and i=l for low doped, LD). The potential distribution in the silicon film in the two regions is approximated by a simple parabolic function in the radial direction as proposed by Young [3] :

$$\phi_i(r,z) = C_{0i}(z) + C_{1i}(z)r + C_{2i}(z)r^2 \tag{2}$$

Applying the boundary conditions [4] we get:

$$\frac{d^2\phi_{si}(z)}{dz^2} + \frac{\phi_{gsi} - \phi_{si}(z)}{\lambda_{cyl}{}^2} = \frac{qN_{ai}}{\varepsilon_{si}} \tag{3}$$

where, ϕ_{gsi}=V_{gs}-V_{Fbi} is the gate potential, ϕ_{si} and V_{Fbi} are the potential at the surface of Si film and the flatband voltage, in the high and low doped regions respectively, λ_{cyl} is the characteristic length for CGT/SGT MOSFET and is given as:

$$\lambda_{cyl} = \sqrt{\varepsilon_{si} t_{si}{}^2 \ln(1 + 2t_{ox}/t_{si}) / 8\varepsilon_{ox}} \tag{4}$$

t_{si} is the silicon film thickness and t_{ox} is the oxide layer thickness. The above equation yields the following solution:

$$\phi_{sh}(z) = A\exp\left(-z/\lambda_{cyl}\right) + B\exp\left(z/\lambda_{cyl}\right) - \sigma_h \tag{5}$$

$$\phi_{sl}(z) = C\exp\left(-(z-L_1)/\lambda_{cyl}\right) + D\exp\left((z-L_1)/\lambda_{cyl}\right) - \sigma_l \tag{6}$$

Where $\sigma_i = \left(qN_{ai}\lambda_{cyl}{}^2/\varepsilon_{si}\right) - \phi_{gsi}$

Let $g_1 = (L_1 + L_2)/\lambda_{cy}$

$$g_2 = \exp\left((L_1 + L_2)/\lambda_{cyl}\right)$$

$$g_3 = 2\phi_{fh} + c1$$

$$g_4 = 1 - \exp\left[2(L_1 + L_2)/\lambda_{cyl}\right]^{-1}$$

$$g_5 = \cosh\left(L_2/\lambda_{cyl}\right)$$

$$V'_{bi} = V_{bi} + V_{ds} + \rho$$

$\rho = \sigma_l - \sigma_h/2$ and $d_1 = qN_{ai}\lambda^2/\varepsilon_{si}$

Using the conditions of continuity of potential and electric field, the coefficients have been evaluated as follows:

$$A = \left[V'_{bi} - (V_{bi} + \sigma)\exp(g_1) - (\rho - \sigma)g_5\right]\exp(g_1)g_4 \tag{7}$$

$$B = \left[(V_{bi} + V_{ds}) - V'_{bi}\exp(g_1) + (\rho - \sigma)g_5\right]\exp(g_1)g_4 \tag{8}$$

$$C = A\exp\left(-L_1/\lambda_{cyl}\right) + \rho \tag{9}$$

$$D = B\exp\left(L_1/\lambda_{cyl}\right) + \rho \tag{10}$$

The position of minimum surface potential ϕ_{shmin} is obtained from (3) as:

$$z_{\min} = \left(\lambda_{cyl}/2\right)\ln\left(A/B\right) \tag{11}$$

The minimum surface potential is then calculated as:

$$\phi_{\mathrm{sh\,min}} = 2\sqrt{\mathrm{AB}} - \sigma \tag{12}$$

The electric field component in the z direction for the high and low doped region is obtained by differentiating (5) and (6) with respect to z as.

$$E_H(z) = \frac{d\phi_{sH}(z)}{dz} = \frac{-A}{\lambda_{cyl}}\exp\left(\frac{-z}{\lambda_{cyl}}\right) + \frac{B}{\lambda_{cyl}}\exp\left(\frac{z}{\lambda_{cyl}}\right) \tag{13}$$

$$E_L(z) = \frac{d\phi_{sL}(z)}{dz} = \frac{-C}{\lambda_{cyl}}\exp\left[\frac{-(z-L_1)}{\lambda_{cyl}}\right] + \frac{D}{\lambda_{cyl}}\exp\left[\frac{z-L_1}{\lambda_{cyl}}\right] \tag{14}$$

Threshold Voltage is obtained from (9) as:

$$V_{th} = \left(-b + \sqrt{b^2 - 4ac}\right)/2a \tag{15}$$

Where, $a = \exp(g_1) - \sin^2 h(g_1) - 2 + g_2$

$\mathrm{b} = \omega\{1 - \mathrm{g}_2\} + 2\mathrm{g}_3\sin^2\mathrm{h}(\mathrm{g}_4) - \delta\{1 - \mathrm{g}_1\}$

$$c = \omega\delta - (g_3)^2 \sin^2 h(g_4)$$
$$\omega = V_{bi}\{1 - g_1\} + V_{ds} - (c1_l - c1_h)g_6 + c1_l - c1_h g_1$$
$$\delta = V_{bi}\{g_2 - 1\} - V_{ds} + (c1_l - c1_h)g_6 - c1_l + c1_h g_2$$
$$c1_i = d_1 + V_{Fbi}$$

RESULTS AND DISCUSSION

The analysis was done keeping N_h=10^{23}m^{-3} and N_l=10^{22}m^{-3}. The oxide thickness was taken as 20nm. Fig.2 shows the variation of surface potential with channel length for different drain voltages. It can be seen that in the HD region, there is no appreciable change in the potential even as drain bias is increased. Also no significant change is noticed in the position of minimum surface potential with increasing drain voltage. This indicates that DIBL effect is suppressed for a GC device. In Fig.3, the variation of electric field along the channel is shown for two different drain voltages. A high doping near the source end results in an increase in the electric field at the source side. It can also be seen that with increase in the drain bias, the field is redistributed mainly at the drain side. In Fig.4, the variation of surface potential with channel is shown for different combinations of the lengths of two regions, keeping the total length constant. It is found that as the length of the HD region is reduced, the point of minimum surface potential shifts towards the source. Due to this, peak electric field will shift more towards the source end resulting in a greater uniformity in the electric field in the channel. The variation of V_{th} with channel length is shown in Fig.5. The results obtained from the model are compared with those obtained for a uniformly doped CGT/SGT [3]. It is evident that V_{th} roll-off has been considerably reduced by using a GC device**.**

CONCLUSION:

An analytical model for GC fully depleted cylindrical/surrounding gate MOSFET is developed. It has been found that a step doping profile in the channel effectively suppresses the SCEs. The shift in the position of minimum surface potential was negligible even when drain bias was increased. The V_{th} roll-off was also considerably reduced. Therefore, it has been established that the laterally asymmetric design effectively suppresses the SCEs such as V_{th} roll-off and DIBL.

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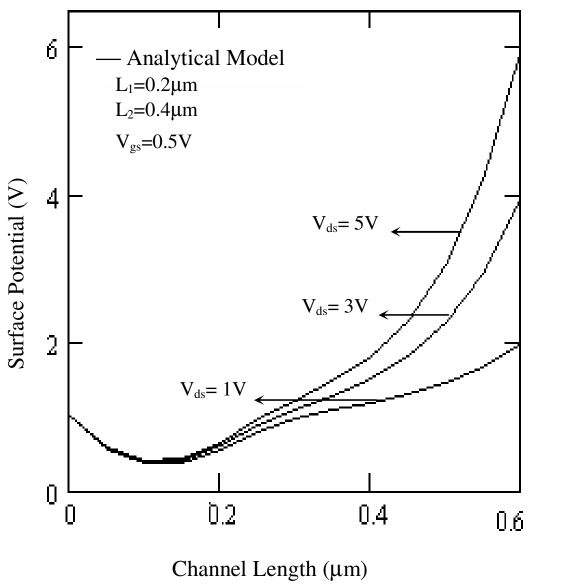

Fig.2 Variation of surface potential with channel length for different drain biases.

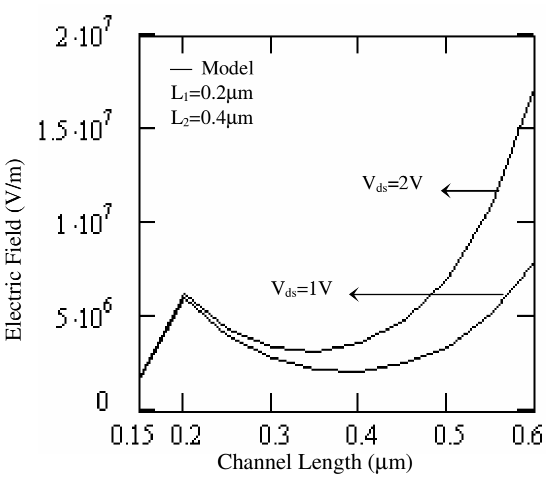

Fig.3 Variation of Electric field with channel length for different drain biases

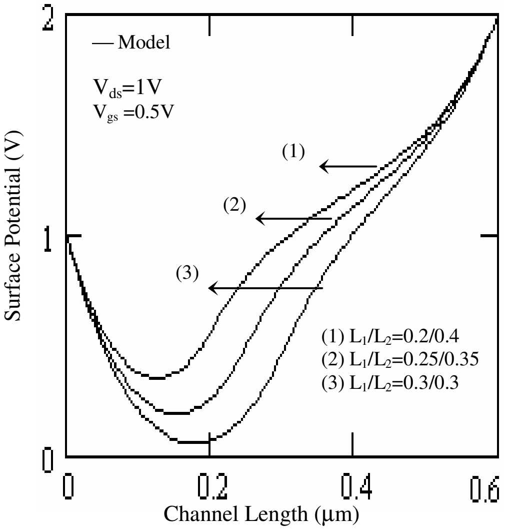

Fig.4 Variation of Surface Potential with channel length for different combinations of L_1 and L_2

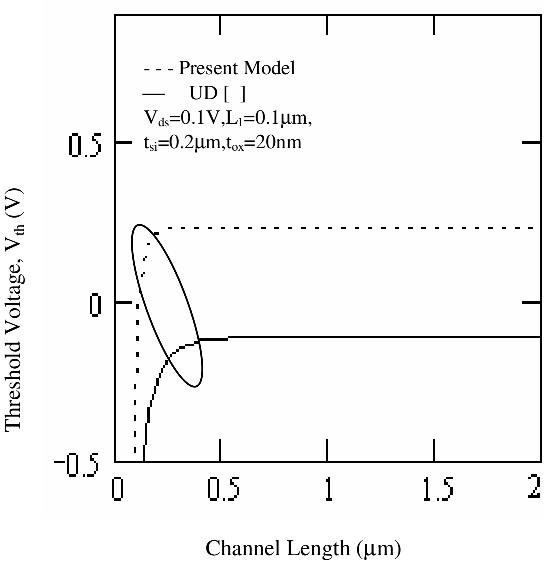

Fig.5 Variation of threshold voltage with channel length for a GC and UD device