# Studies on the Electrical Characteristics of Ni and NiPt-alloy Silicided Schottky Diodes

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## ABSTRACT

Ni(Pt) alloy-silicided/$Si_{1-x}Ge_x$ Schottky barrier diodes have been fabricated by annealing the co-deposited NiPt alloy film on $Si_{1-x}Ge_x$ layers and characterized electrically in the temperature range of 100 K-300 K to investigate the effect of Pt co-deposition (with Ni) on the electrical characteristics of alloy-silicided Schottky diodes. The Schottky barrier height ($\phi_b$) and ideality factor ($\eta$) have been determined from the surface potential-voltage ($\Psi_s$-V) plot and the $\phi_b$, extracted from capacitance-voltage (C-V) characteristics, has been compared with the barrier height evaluated from thermionic emission model. It has been found that the barrier height values extracted from the $\Psi_s$-V and C-V characteristics are different, indicating the existence of an in-homogeneous Schottky interface. The I-V characteristics have also been simulated using SEMICAD device simulator to model the alloy-silicided Schottky diode with non-ideal interface. An interfacial layer, a series resistance and modified work function of silicide material were included in the diode model to achieve a better agreement with the experimental data. Results are also compared with Ni-silicided/SiGe Schottky diode processed in the same run. The variation of electrical properties between the Ni(Pt)/SiGe and Ni/SiGe Schottky diodes has been attributed to the presence of Pt at the silicide-SiGe interface, which may enhance the thermal stability and increase sheet resistivity of the silicided layer.

## INTRODUCTION

Schottky contacts play an important role in controlling the electrical performances of semiconductor device and Schottky barrier height (SBH), which is highly sensitive to the thermal treatment of the metal-semiconductor interface, is one of the crucial parameters in this context. Since last decade, the applications of SiGe material system are increasing due to its potential to deliver high speed and high performance electronic and optoelectronic devices. Furthermore, due to its compatibility with the existing Si technology, the SiGe heterostructures have attracted considerable attention for the fabrication of both the electronic and optoelectronic device. All these devices need a good and reliable contact for their successful operation. Moreover, the contacts for high performance devices, ultra large scale integrated (ULSI) circuits and interconnects require silicides which are thermally stable, low resistive, and compatible with the process technology [1]. Nickel-silicide (NiSi) is a promising silicide material being investigated so far due to its low formation temperature (<500°C), low Si consumption during silicidation and low contact resistance [2]. Self-aligned silicidation has become an important part of the ULSI technology because a low resistivity must achieve for the source, drain and poly-silicon gate interconnects to reduce RC delay. But one potential problem for Ni-silicide is the nucleation of high resistive phase, particularly at high temperature. To overcome this problem and modify the process window for defect free silicidation, new types of metal-silicides are required.

Ni(alloy)-silicides have recently gained much attention due to their improved properties, which can be adapted in advance complementary metal oxide semiconductor (CMOS) technology. Among different alloy silicides, Ni(Pt) has shown enhanced functionality in sub-micron devices. Also the formation of NiSi-induced defects in silicon during silicidation is an important issue that prompt the fabrication and analysis of Ni(Pt) alloy silicide material as the new generation contact material for ULSI interconnects. It has also been reported that the incorporation of small amount of Pt (5%-10%) during Ni co-deposition may enhance the thermal stability of Ni-silicides due to the formation of pseudo-binary solid solution [3]. Thus it seems that the use of Ni(Pt)-alloy silicide is desirable for deep

sub-micron CMOS technology, although one major problem is the increased sheet resistivity due to the agglomeration of the thin Ni(Pt)Si during annealing.

In this work we report on the results of our analyses and the electrical measurements of Ni(Pt)-alloy silicided Schottky diodes. The effect of the addition of a small amount of Pt (typically ~ 5%) on the electrical characteristics of silicide Schottky diodes has been studied. Current–Voltage (I-V) characteristics of the diodes were measured and simulated with modified mobility and metal work function, to investigate the alloyed interface. The temperature dependence of the barrier height ($\phi_b$) and ideality factor ($\eta$) have been determined. The electrical properties of a co-processed Ni-silicide/SiGe Schottky diode are also included for comparison.

**EXPERIMENTAL**

The starting wafer was a 4 inch Si (100) substrate ($N_d = 1.5 \times 10^{16}$ $cm^{-3}$). After the growth of 3μm thick $Si_{1-x}Ge_x$ graded layer (x~0.0-0.3), a 1.5μm thick relaxed $Si_{1-x}Ge_x$ (x~0.3) buffer layer was also grown on top of the compositionally graded $Si_{1-x}Ge_x$ (x=0~0.3) layer by using ultra high vacuum chemical vapor deposition (UHVCVD) system. The growth temperature was 900 °C while the system pressure was maintained about 25 mTorr. After removing the native oxide using a piranha followed by HF dip, 10 nm thick Ni films were deposited at room temperature on the $Si_{0.7}Ge_{0.3}$ buffer layers, using a single electron beam evaporator. Similarly, 10 nm thick NiPt (Ni~95% and Pt~5%) alloy films were co-deposited and patterned on $Si_{0.7}Ge_{0.3}$ buffer layer by means of dual electron beam evaporator at a pressure $3 \times 10^{-3}$ Torr. The details of the growth conditions and the characterization of the relaxed SiGe films can be found elsewhere [4]. The silicidation and inter-diffusion was carried out by using a rapid thermal processing system in the temperatures range of 400–500°C for 60 s in $N_2$ ambient. After silicidation, unreacted metal was removed using a $H_2SO_4$:$H_2O_2$ solution. The schematics of the structures before silicidation are shown in Fig.1. The I-V and C-V characteristics were measured by using HP-4140B picoammeter and HP-4061A semiconductor component test system, respectively.

**RESUALTS AND DISCUSSION**

The logarithmic I-V characteristics of the Ni/$Si_{0.7}Ge_{0.3}$ and NiPt(~5%)/$Si_{0.7}Ge_{0.3}$ Schottky diodes measured at different temperatures are shown in Figs. 2(a) and 2(b). A good rectifier regime is observed in silicided Schottky diodes. Results indicate that the temperature independent slopes of I-V curves and deviation from linearity at higher voltages may occur due to the presence of series resistance ($R_s$). Figs. 2(a) and 2(b) also shows that the reverse saturated current across the NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diode is higher than the Ni/$Si_{0.7}Ge_{0.3}$ Schottky diode. This is attributed to the difference that appears at the interface of the silicided Schottky diode. In absence of a Pt, Ni reacts directly with $Si_{0.7}Ge_{0.3}$ resulting in a non-uniform interface due to segregation of Ge atom at the silicide-semiconductor interface [5]. The I-V characteristics of the NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diodes were simulated using SEMICAD device simulator, to understand the alloy silicide interface. In device simulation, the Schottky boundaries have been modeled by incorporating the image force lowering, thermionic emission and modified alloy silicide work function. The simulated I-V characteristics for alloy-silicided Schottky diodes at temperatures 200 K, 250 K and 300 K are shown in Fig. 3. From Fig. 3, one observes that the simulated results provide an excellent quality fit at both forward and reverse bias, except at the reverse bias measured at a very low temperature. In this temperature range, the edge leakage and generation recombination current is quite effective [6] which have not been considered in the present model.

Ni has a smaller atomic size and lower melting point than Pt and thus it should diffuse more rapidly towards SiGe epi-layer, and results in the formation of a complex mono-germanosilicide phase. To overcome this non-uniformity at the interface, a limited quantity of Pt is incorporated and co-deposited with Ni during metal deposition. The requirement for as-deposited NiPt alloy would lead to the formation of higher order silicides compared to Ni film grown on $Si_{0.7}Ge_{0.3}$ and prevent Ge segregated as Ni(SiGe) at interface[7]. The NiPt alloy formed decisive compound NiPt(SiGe) silicide, which is a very high resistive alloyed silicide phase (formed at 400 °C annealing temperature) but one important aspect is that the phase is thermally stable[8]. Due to the incorporation of small amount of Pt during Ni-silicidation process, unwanted spiking of silicides is reduced and the thermal stability of the film is also enhanced. Moreover, silicided diodes with a Ni(Pt) alloy, showed good I-V characteristics without any non-ideal features of the Schottky contact.

The surface potential $\Psi_s$ was evaluated from the experimental I–V data by using the following relation [6].

$$J = A^* T^2 \exp\left(-qV_n / KT\right) \exp\left(-q\Psi_s / KT\right) \quad \dots (1)$$

where A* is the effective Richardson constant, T the temperature in Kelvin scale, $qV_n$ the energy difference between the conduction band and the Fermi level and $\Psi_s$ is the surface potential and is plotted in Fig. 4 as a function of applied bias. From Fig. 4, it is observed that the surface potential decreases linearly up to a critical point ($J_c$, $V_c$) after which the effect of series resistance plays a crucial role to modify the I-V characteristics as well as the surface potential-bias

voltage ($\Psi_s$-V) plot. Fig. 4 indicates that the Pt incorporation may increase the surface potential due to the formation of interface states.

The Schottky barrier height ($\Phi_b$) and ideality factor ($\eta$), which control the carrier propagation across the barrier of a Schottky diode, have been extracted from $\Psi_s$-V characteristics in the temperature range 100 K–300 K by using following relations [9].

$$\Phi_b = \Psi_s(J_c, V_c) + \frac{V_c}{\eta} + V_n - \frac{KT}{q} \quad \ldots(2)$$

where, $-\frac{1}{\eta} = \left(\frac{d\Psi_s}{dV}\right)_{J_c, V_c}$ and $\frac{R_s}{\eta} = \left(\frac{d\Psi_s}{dJ}\right)_{J_c, V_c}$

The variation of ideality factor with measuring temperature of $NiPt/Si_{0.7}Ge_{0.3}$ and $Ni/Si_{0.7}Ge_{0.3}$ is shown in Fig.5. From Fig. 5, one observes that the non-idealities are dominant at low temperature for both the diodes. But at room temperature, alloy silicided Schottky diode shows nearly ideal behavior compared to $Ni/Si_{0.7}Ge_{0.3}$ Schottky diode. Fig. 6 demonstrates that the barrier height of $NiPt/Si_{0.7}Ge_{0.3}$ Schottky diode is temperature independent while the barrier heights of Ni/Si0.7Ge0.3 diode increase rapidly with increasing temperature. The barrier height measured at room temperature for $Ni/Si_{0.7}Ge_{0.3}$ and $NiPt/Si_{0.7}Ge_{0.3}$ Schottky diode are 0.671 eV and 0.692 eV, which is attributed to the higher work function of the Ni(alloy) silicides. To reduce the silicon consumption at the expense of higher sheet resistance in this context, Pt alloying with Ni-silicidation is performed. Alloy-silicides may reduce the surface-inhomogeneity in consequence of which the leakage current is reduced drastically. Hence, the variation of barrier height of $NiPt/Si_{0.7}Ge_{0.3}$ Schottky diode is nearly stable with increasing temperature.

The barrier height was also calculated from the reverse C-V characteristics. The calculated barrier height at room temperature for $Ni/Si_{0.7}Ge_{0.3}$ and $NiPt/Si_{0.7}Ge_{0.3}$ are 0.68 eV and 0.699 eV, respectively. The variation of barrier height obtained from $\Psi_s$-V and C-V curves is attributed to the presence of interface states and partly due to the injected minority carriers from the back contact. The effect is enhanced in $Ni/Si_{0.7}Ge_{0.3}$ Schottky diode due to the uncontrolled silicidation at the interface. The increase in barrier height of Ni(Pt) silicide is attributed to the penetration of Pt towards silicide semiconductor interface. The capacitance per unit area ($C_D$) of a reverse biased Schottky diode can be expressed as [6].

$$C_D = \sqrt{\frac{q\varepsilon_s N_d}{2\left(V_{bi} - V - K_B T / q\right)}} \quad \ldots(3)$$

where $\varepsilon_s$ is the relative permittivity of the semiconductor, $N_d$ the donor concentration, V is the applied reverse bias and $V_{bi}$ the built in potential. Figs. 7(a) and 7(b) show the typical $1/C_D^2$ vs. applied bias plot for the $Ni/ Si_{0.7}Ge_{0.3}$ and $NiPt/Si_{0.7}Ge_{0.3}$ Schottky diodes, respectively. The barrier height is calculated by using the following relation [6].

$$\phi_b = \frac{k_B T}{q} + V_n + V_i \quad \ldots(4)$$

where $V_i$ is extracted from the intercepts on the voltage axis (X-axis) of Figs. 7(a) and 7(b) and $V_n$ is the energy difference between Fermi level and conduction band. The intercept voltage ($V_i$), obtained from the reverse C-V ($1/C_D^2$-V plot) characteristics is 0.549 V and 0.568 V for the $Ni/Si_{0.7}Ge_{0.3}$ and $NiPt/Si_{0.7}Ge_{0.3}$ Schottky diodes, respectively, and the corresponding barrier heights are 0.680 eV and 0.699 eV. The capacitance method is found to give barrier height that differs significantly from those obtained from the $\Psi_s$ -V characteristics. This is specifically true when there is an interfacial layer present and the barrier height changes with applied bias. It is clear from Fig. 7(b) that the plot of $C^{-2}$ against applied bias is a perfect straight line indicating that there is no appreciable interfacial layer in the alloy-silicide semiconductor interface due to the addition of Pt within Ni silicide. Consequently, the reverse $C^{-2}$ vs. applied bias curve of $Ni/Si_{0.7}Ge_{0.3}$ Schottky diode clearly indicates that the interface is not free from Ge segregation. Table-1 shows the Schottky barrier heights obtained from $\Psi_s$-V and C-V characteristics. The deviations in the results is prominent for $Ni/Si_{0.7}Ge_{0.3}$ Schottky diodes and it can be analyzed and correlated with the presence of in-homogeneity, deep impurity levels and edge leakage current at the interface. This discrepancy can also be explained by considering the existence of an interfacial layer or trap states in the silicide-semiconductor interface.

## CONCLUSION

In summary, we have measured, simulated, and compared the I-V characteristics of Schottky diodes silicided with Ni and Ni(Pt) alloy. Good I-V characteristics were observed for all the diodes except for some of the Ni-silicided diodes, which showed a reverse saturated I-V characteristics. Barrier height and ideality factor are also extracted from the measured $\Psi_s$-V characteristics and they are also found to be temperature dependent. It is found that ideality factor decrease with temperature while the barrier height increases slowly with temperature for the $Ni(Pt)/Si_{0.7}Ge_{0.3}$ Schottky diodes and rapidly for $Ni/Si_{0.7}Ge_{0.3}$ Schottky diodes. Experimental I-V characteristics are also compared with the simulation to investigate the effect of Pt addition during Ni-silicidation. Ni(Pt) alloy-silicided diodes showed a good I-V characteristics without any evidence of non-ideal Schottky interface at all temperature. Results indicate that the thermal stability of NiSi may enhance due to the Pt co-deposition. In order to be compatible

with the scaling down of junction depths in CMOS devices, silicide thickness need to be scaled down proportionately and control of the Si consumption at the expense of a higher sheet resistance of silicides.

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**Table 1. Comparative Barrier height measured at 300 $^{o}$C**

| Diode structure | Barrier height from $\Psi_s$ –V (eV) | Barrier height from C –V (eV) |
|---|---|---|
| Ni/$Si_{0.7}Ge_{0.3}$ | 0.671 | 0.681 |
| NiPt/$Si_{0.7}Ge_{0.3}$ | 0.692 | 0.69 |

**Figure Captions**

Fig.1. Schematics of the structures for Ni/$Si_{1-x}Ge_x$ (x=0.3) and NiPt(~5%)/$Si_{1-x}Ge_x$ (x=0.3) Schottky diodes.

Fig.2. I-V characteristics at different temperatures (100 K, 150 K, 200 K, 250 K, and 300 K) of (a) Ni/$Si_{0.7}Ge_{0.3}$ Schottky diodes and (b) NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diodes.

Fig.3. Simulated I-V characteristics for NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diodes at different temperatures (200 K, 250 K, 300 K).

Fig.4. Variation of surface potential ($\Psi$s) with applied bias (V) for Ni/$Si_{0.7}Ge_{0.3}$ and NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diodes. The dashed line indicates the variation of $\Psi$s in absence of a series resistance ($R_s$).

Fig.5. Variation of ideality factor $\eta$ of Ni/$Si_{0.7}Ge_{0.3}$ and NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diodes as a function of temperature.

Fig.6. Variation of barrier height $\Phi_b$ of Ni/$Si_{0.7}Ge_{0.3}$ and NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diodes as a function of temperature.

Fig.7. Plot of $1/C_D^2$ vs. applied bias (V) of (a) Ni/$Si_{0.7}Ge_{0.3}$ and (b) NiPt/$Si_{0.7}Ge_{0.3}$ Schottky diodes at room temperature.

**Figures:**

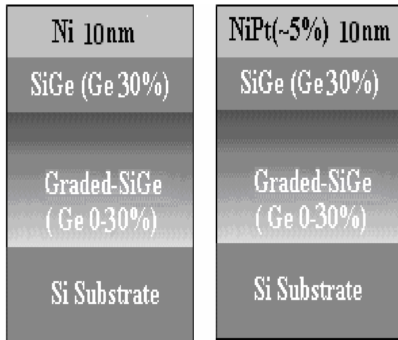

Fig. 1.

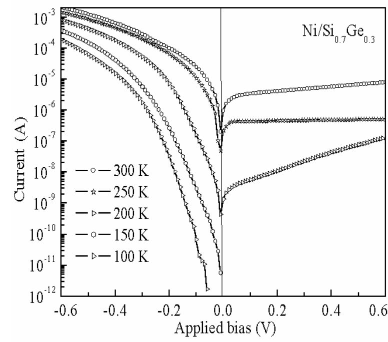

Fig. 2(a).

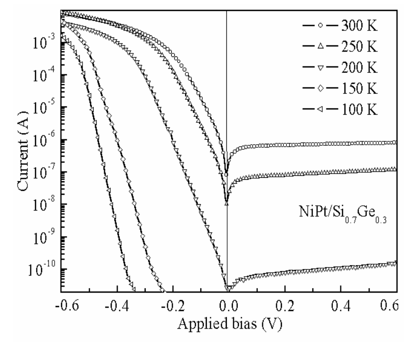

Fig. 2(b).

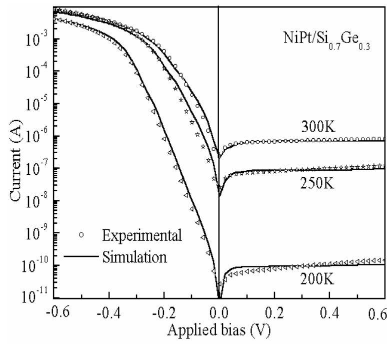

Fig. 3.

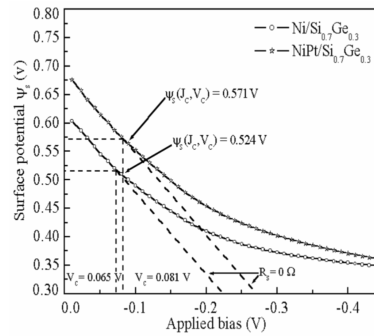

Fig. 4.

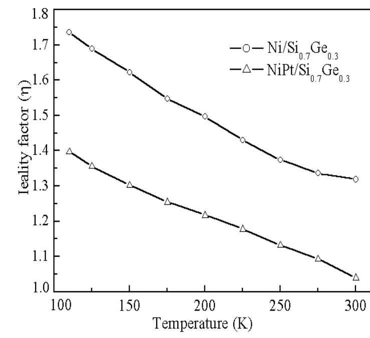

Fig. 5.

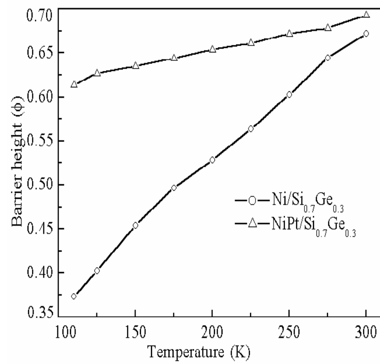

Fig. 6.

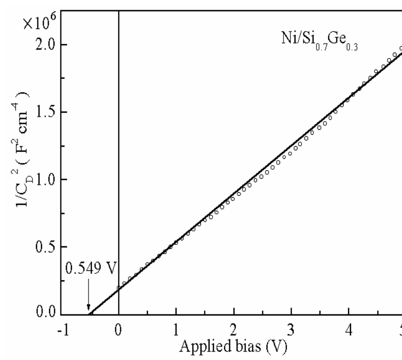

Fig. 7(a).

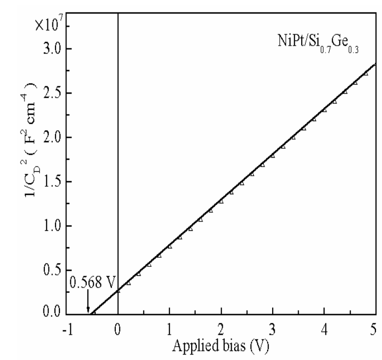

Fig. 7(b)