Low Temperature Co-fired Ceramic (LTCC) Technology for RF Multi-layer Circuit Applications-Technology and Modeling

Aly E Fathy

ECE DEPARTMENT, UNIVERSITY OF TENNESSEE, KNOXVILLE, TN 37996, USA.
FATHY@ECE.UTK.EDU

ABSTRACT:

Mixed signal RF wireless products require the development of a low cost multi-layer, multi-chip packaging technology. LTCC has matured in the last few years, and it is optimum for this application. Examples of manufacturing approaches and design libraries are shown here with a few examples to demonstrate its enabling power.

I- INTRODUCTION:

Mixed signal designs of RF products still require major performance improvement and size-reduction. They tend to use up a large number of passive components, and the vast majority of these products use surface mount discrete parts. They require a sizable percentage of the printed circuit board area which greatly limits their size miniaturization and RF performance. Additionally, these component assembly cost is a major component of their prices.

The 3D integration of all the dc power lines, analog circuits, high-speed digital logic circuits, and RF/microwave components into a multi-layer environment has become the trend and a common target for many of these mixed-signal products. Small size, lower cost, better performance, and higher reliability can be achieved by embedding passive components during substrate manufacture. LTCC technology has been demonstrated to be optimum for low cost RF multi-layer applications.

LTCC technology can be tailored to provide controlled sintering *during the firing operation allowing the accurate placement of embedded components such as resistors, capacitors, transmission lines, etc* [1].

This overview paper touches upon the development of such technology and its utilization in building various surface and embedded components for various wireless circuits and packaging applications. The paper discusses some of the demonstrated complex mixed signals prototypes that have been already demonstrated in the market and emphasizes the strength of this enabling technology.

II- TECHNOLOGY DEVELOPMENT GOALS:

Over the last several years, the customer-driven wireless market has pushed the developers of RF hardware towards more functionality in less volume, operation at ever-higher RF frequencies, and greater circuit and functional integration. Additionally, the pressure to reduce costs has forced designers to look at less expensive manufacturing, assembly, and testing techniques.

Multilayer and multichip system integration techniques have been realized in many different formats, each with its own strengths and weaknesses. Best performance is generally obtained using hybrid technology on high temperature ceramics, while lowest cost is often achieved with several of the organic (or "soft") board technologies [2].

Low Temperature Cofired Ceramic (LTCC) technology has been used to deliver both high performance and low cost. In its basic version, however, it suffers from two major drawbacks. First, the ceramic shrinks after firing in all three dimensions. This limits the size of the boards that can be processed, imposes limitations on embedded passive components, and introduces complexity in the processing of boards with cavities. Second, modules requiring heat removal must have a heat spreader attached after firing. Researchers have already developed various techniques to control this shrinkage problem, appropriate design rules, and the knowledge to account for LTCC processing and shrinkage control [1,2].

III- EXAMPLES OF MANUFACTURING APPROACHES:

Sarnoff, for example, has developed an approach called Low Temperature Cofired Ceramic on Metal[i] (LTCC-M), in which a specially formulated multilayer ceramic structure is attached to a metal carrier or

"core". The ceramic firing and core attachment process occur in one and the same step. The resulting structure exhibits virtually no shrinkage in the plane of the substrate. All the shrinkage is constrained to the Z dimension (normal to the plane of the substrate). The Z dimension shrinkage is very predictable and uniform. Fig. 1 is a flow diagram of the fabrication process. The process allows the inclusion of buried resistors and overlay capacitors covering a wide range of values, as well as vias and planar conductor patterns such as

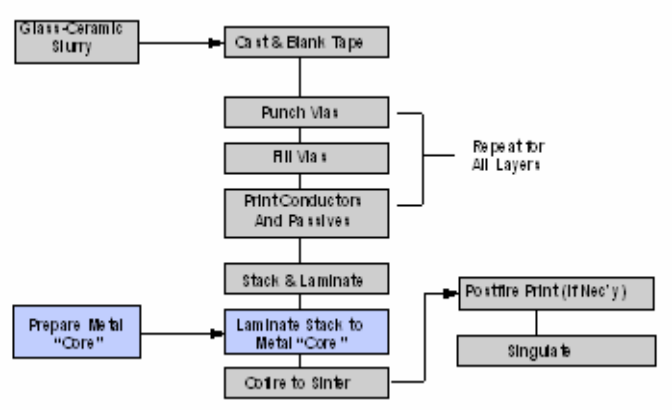


Figure 1: Flow Chart of the LTCC-M Processing step.

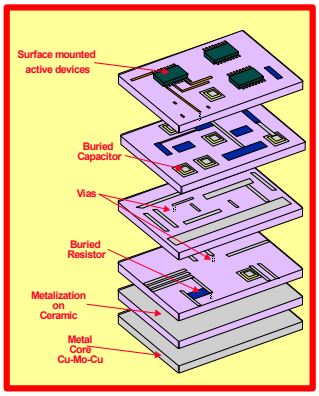


Figure 2: LTCC-M technology capabilities.

transmission lines and spiral inductors. The virtual absence of shrinkage in the X-Y plane allows the fabrication of relatively large area boards with excellent layer-to-layer registration and alignment accuracy. Fig. 2 illustrates the cross-section of a typical single-sided board, including the metal core, vias, and surface-mounted components. Depending on the application, various metals can be used for the core. For RF applications, Sarnoff has developed two systems, one based on a Cu-Mo-Cu laminate and the other on Kovar. The Cu-Mo-Cu core is preferred for applications in which maximum heat removal is required. Cu-Mo-Cu metal laminate also has an expansion coefficient, which closely matches that of GaAs, allowing the mounting step of bare die directly on the heat spreader [1].

Another examples is the TDK[ii] process. TDK has developed proprietary high performance materials. Their process allows mixed dielectric substrates co-firing, and utilize laser-drilled vias to avoid stacking issues. It includes modules and integrated passive arrays. Meanwhile, Dupont[iii] has developed an industry standard green tape material for general-purpose applications. Their process includes dielectric, signal conductors, via fill conductors, wire-bondable or solderable surface conductors, braze material, resistor material, capacitor material, and overglaze. Dupont process utilizes screen printable or photo-imaging conductors. Some of their tapes have demonstrated low loss and their use have been extended beyond 70 GHz.

IV- EMBEDDED RF LUMPED ELEMENTS:

Many vendors have optimized their processes to embed lumped elements. Capacitor inks are required to have dielectric constants values ranging from 10 to few thousands and should exhibit low temperature coefficients of capacitance (TCC). These values, in general, allow integrated capacitors to span the range from 0.2 to 50,000 pF. Typical capacitor tolerances are currently in the range of ±(10 –20)%.

In addition, to meet various system requirements, a series of buried resistor ink compositions need to be developed with sheet resistivity in the range of few ohms per square to several KΩs per square. Developed inks should exhibit low temperature coefficients of resistance (TCR). Typical buried resistor absolute tolerances are currently in the range of ±(15 – 25)%, while tighter relative tolerances can be achieved for resistor divider networks of less than ±5%.

V- LTCC DESIGN LIBRARIES:

In order to make this technology more accessible and easier to use, manufacturing companies have developed special design libraries. These simulation and layout tools of the multilayer LTCC substrates contain embedded models for lumped passive components, surface transmission lines, embedded transmission lines, and vias [2]. The included design rules incorporate materials parameters such as ceramic dielectric constant, ink parameters, metallization thickness, etc. These CAD models enable the circuit designer to function in a multilayer environment and support integrated passive components. Models validation is a must to accept these library models. Examples of using Sarnoff's developed software package to validate lumped element models are shown in Fig. 3. Sarnoff's models [2] are based on Agilent's communication design suite package. However, similar commercial packages have been developed recently such as that of Ansoft[iv] and

Agilent[iii].

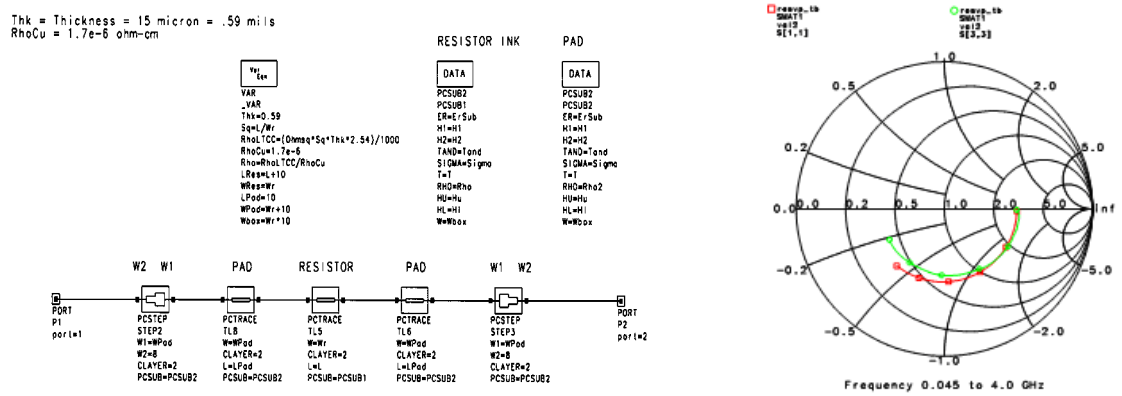
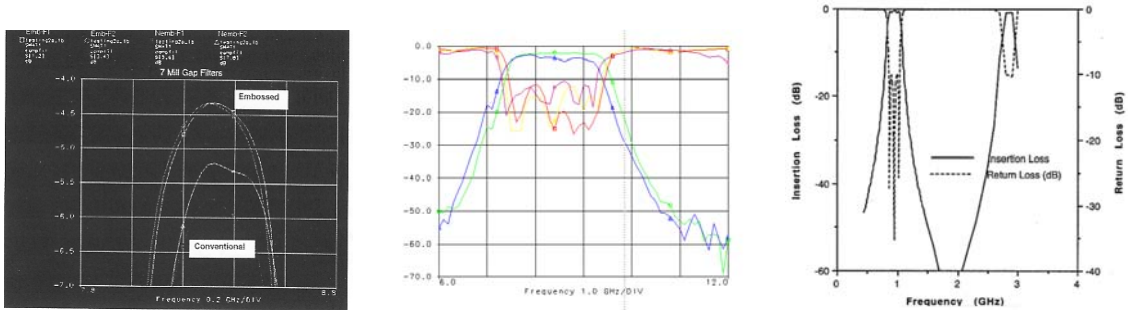


Figure 3: Example of Models Validation: Sarnoff's resistor library model; and its simulated and measured results.



a. b) c)

Figure 4: a) Performance of a narrow band pass filter design, b) Measured and predicted LTCC band pass filter. c) Measured performance of an embedded image reject filter.

VI- TECHNOLOGY EVALUATION

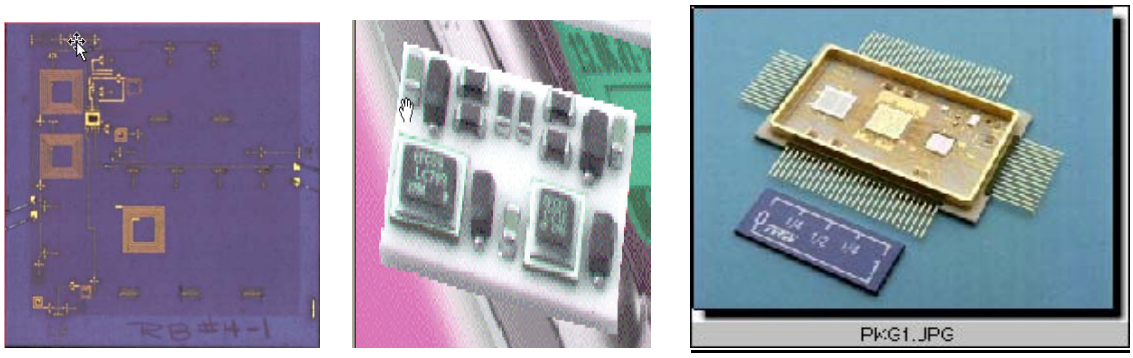
Filter structures are used to evaluate the effects of various metallization inks, and define all surface as well as embedded transmission lines. A microstrip filter was designed and fabricated on the top surface of LTCC structure that consisted of a series of coupled lines. Minimum line spacing and width can be determined from such evaluation. It was found that embossing of these lines would render better-defined lines, and much smoother edges. Fig. x indicates that significant insertion loss improvement can be achieved by embossing these coupled lines. Finer line definition can be utilized using advanced lithographic techniques only on the top surface, but they are relatively expensive.

VII- EXAMPLES OF COMPLICATED SUB-SYSTEMS:

A direct digital synthesizer (DDS) was designed, fabricated, and tested in a joint effort between Sarnoff, TRW, and DLI. Fig. 4a shows a fabricated prototype, where the module includes two cavities and 82% of all passive components are buried. The module is comprised of 9 tape and 10 conductor layers. Wire-bonding was utilized for active devices attachment. The DDS prototype operated successfully over 500MHz clock frequencies and its peak harmonic distortion was demonstrated to be better than –69 dBc.

The EPCOS[v]'s world's smallest front-end module (FEM) for GSM triple band mobile service is another excellent example (shown in Fig. 5b). Its LTCC implementation integrates more than 50 components in a package measuring only 6.7x5.5x1.8 mm. Its design reduces the board space requirements by 95% as compared to conventional design with discrete components. Many other excellent examples have been introduced as well in the market demonstrating the enabling power of this RF multi-layer low cost packaging technology. Other demonstrated applications include full GSM RF front end as seen in Fig. 5a.

.



a) b) c)

Figure 5: a) LTCC implementation of a wireless RF front-end b) the DDS package c) The EPCOS smallest RF front end

VIII- CONCLUSIONS:

LTCC technology has been significantly advanced in the last few years. The technology enables further miniaturization, and the development of compact, reliable, low cost, 3D circuits and integrated packages. Embedding of cavities, RF-passive components, stack of different dielectric layers are a reality today. High performance components that operate at frequencies beyond 70 GHz have been successfully demonstrated[i]. The 3D integration of all the dc power lines, analog circuits, high-speed digital logic circuits, and RF/microwave components into a multi-layer environment has become the trend and a common target for many of these mixed-signal products [4,5].

REFERENCES

[1] Geller, B. Thaler, B. Fathy, A. Liberatore, M.J. Chen, H.D. Ayers, G. Pendrick V., "*Technologies for Wireless Applications*", 1999 Digest, IEEE MTT-S Symp., pp. 189- 192, 1999.

[2] Fathy, et al.., "Design of embedded passive components in Low-Temperature CofiredCeramic on Metal (LTCC-M) technology," *Microwave Symposium Digest*, 1998 IEEE MTT-S Symp., v. 3, pp. 1281-1284， June 1998

[3] Kwang Lim Choi, Nanju Na, and Madhavan Swaminathan, "Characterization of Embedded Passives Using Macromodels in LTCC Technology," *IEEE Transactions on Components, Packing, and Manufacturing Technology—Part B*, vol. 21, No. 3, Auguest 1998.

[3] Fathy, A. Pendrick, V. Ayers, G. Geller, B. Narayan, Y. Thaler, B. Chen, H.D. Liberatore, M.J. Prokop, J. Choi, K.L. Swaminathan, M., "Design of embedded passive components in Low-Temperature CofiredCeramic on Metal (LTCC-M) technology," *Microwave Symposium Digest*, 1998 IEEE MTT-S Symp., v. 3, pp. 1281-1284， June 1998.

[4]. D. Heo, A. Sutono, E. Chen, Y. Suh, and J. Laskar," A 1.9-GHz DECT CMOS Power Amplifier with Fully Integrated Multilayer LTCC Passives," *IEEE Microwave and Wireless Components Letters*, vol. 11, No. 6, pp. 249-251, June 2001,.

[5]. Young Do Kim, Ho-Yong Kim, Hong Min Lee, "Dual-band LTCC chip antenna design using stacked meander patch for mobile handsets," *Microwave and optical technology letters,* Vol. 45, Issue 411, pp. 271-273, April 2005.[i]

---

[i] http://www.laminaceramics.com/

[ii] TDK: http://www.tdkltcc.com/

[iii] 943 Low Temperature Co-Fired Ceramic (**LTCC**) materials. The 943 Design Kit is integrated with the **Agilent** EEsof EDA Advanced Design System (**ADS**).http://www.dupont.com/mcm/product/943design.html

[iv] Ansoft Designer http://www.ansoft.com/news/articles/03.09_MWRF.pdf

v EPCOS: http://www.epcos.com/web/applications/html/ltcc_techonology.html