SOFTWARE DEFIEND PHASE LOCKED LOOP

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ABSTRACT

In this paper a new variety of the digitized version of an analog phase locked loop has been proposed in order to overcome the conditionally stable nature of a software controlled phase locked loop. Also the conventional need of a low pass filter to filter out the high frequency components at the output of a phase detector is avoided through the use of In-phase and Quadrature signals. MATLAB simulation results have been presented in support of the conclusions of the analyses.

INTRODUCTION

Due to the development of VLSI technology it has become popular to use high speed DSP LSI chips for realizing digitized version of a phase locked loop, the most prolific feedback control system, being used in every cell phone, computer, pager, telephone, communication receivers, television, etc. As such a need has been felt to develop a phase locking arrangement that can overcome the weakness of a conventional phase locked loop (PLL), namely, loop-parameter sensitivity of a PLL. This has led to the idea of developing a software version of a PLL where the loop parameters can be easily and quickly changed making the system most suitable for adaptive control system. Although the software version or digitized version of the PLL so far developed removes the weak points of an analog PLL, yet the attempt has ended up with a model the stability of which is extremely susceptible to loop gain. Even the first order digitized version or software controlled PLL is conditionally stable, whereas a first order analog PLL is unconditionally stable. This paper suggests a simple way of overcoming this difficulty to a large extent. The total elimination of the difficulty appears impossible due to the delayed nature of the control.

MECHANIZATION OF THE PROPOSED SYSTEM

A typical configuration where the proposed software defined phase locked loop (SDPLL) is for receiving a high frequency signal is depicted in Fig.1.The circuit –configuration, preceding the SDPLL is arrangement for generating in-

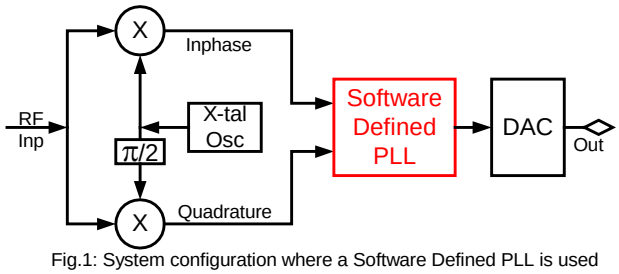

Fig.1: System configuration where a Software Defined PLL is used

phase and Quadrature signals at an appropriate frequency from the rf or microwave signals. This is done in order not to cross the speed limit of DSP-LSI chips. The proposed software defined PLL has all the ingredients of a standard PLL, as shown in Fig.2, namely, a phase detector, the loop filter and voltage-controlled oscillator, but incorporates an additional component (a phase modulator) the modulates the instantaneous phase of the voltage controlled oscillator in correspondence to a measure of the phase error between the input and the output. Another point of difference from the earlier work is that here the I-Q channels of the both the input and the output are used to realize phase detection, The advantages are: no need of an extra filter to remove the high frequency components after phase detection and no transient impairments during operation of the PLL. The voltage-controlled oscillator (VCO) is algorithmically based on the fact that the control voltage, i.e., the phase detector output, is applied to the VCO after one sampling interval.

SYSTEM EQUATION

The In-phase and Quadrature components of the input signal and outputs of the voltage-controlled numerical oscillator are assumed to be of the forms

$$X_i(k) = A\sin\theta(k)$$
$$X_Q(k) = A\cos\theta(k)$$

and (1)

$$W_I(k) = \sin\psi(k)$$
$$W_Q(k) = \cos\psi(k)$$

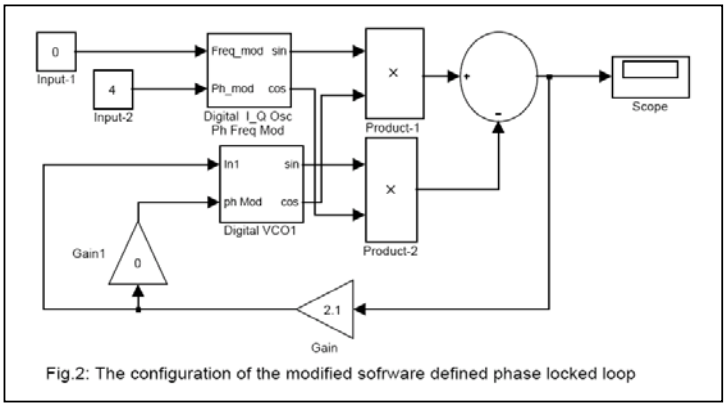

Fig.2: The configuration of the modified sofrware defined phase locked loop

Hence referring to Fig.2 the phase detector output is given by

$$Y(k) = A\sin\varphi(k) \quad (2)$$

Note that

$$\theta(k) = \frac{2\pi f_1 k}{f_s} + \psi_1(k)$$
$$\psi(k) = \frac{2\pi f_2 k}{f_s} + \psi_2(k) \quad (3)$$

Where $\psi_1(k)$ input modulation and $\psi_2(k)$ is given by

$$\psi_2(k) = \psi_2(k-1) + KY(k-1) + K_pY(k-1) \quad (4)$$

If 'K' is the sensitivity of the VCO and 'K_p' is the sensitivity of the phase modulator gain, ϕ(k) is the phase error between the input and output at the k^{th} instant then one obtains the following equations for a first order system

$$\varphi(k) = \theta(k) - \psi(k)$$
$$\phi(k) - \phi(k-1) = \Omega - AK\sin\phi(k-1) - AK_p\left[\sin\phi(k) - \sin\phi(k-1)\right] \quad (5)$$

Where

$$\Omega = \frac{2\pi(f_1 - f_2)}{f_s}$$

In deriving the equation no input phase modulation is assumed. Assume that the initial frequency error is zero. Let us assume that the loop phase error oscillates between two values φ_1, φ_2, φ_3….. then it is easily that φ_1,= φ_2 and hence

$$\frac{\sin\varphi_1}{\varphi_1} = \frac{2}{AK - 2AK_p} \quad (6)$$

This indicates that for stable operation, i.e., non-oscillatory condition it is seen from the above relation

$$AK - 2AK_p \le 2, \textit{i.e.}, AK \le 2(1 + AK_p) \tag{7}$$

This equation clearly demonstrates that the for the proposed software defined PLL the loop gain AK can be much higher than '2' which is the limiting gain of conventional digitized loop for stable operation.

NUMERICAL EXPERIMENT

Simulation results as observed on MATLAB are shown in Fig.3a and Fig.3b.

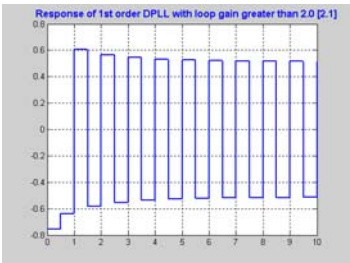

Fig.3a: Showing instability when the loop gain is greater than 2.0

Fig.3b: Showing stable operation with additional phase control

The response of the SDPLL to an FM signal is shown in Fig.4. From the simulation results it is clearly seen that the

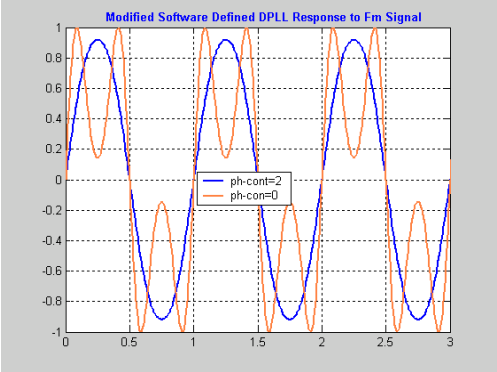

Fig.4: Performance of the SDPLL as demodulator

addition of the phase modulator improves the performance the modified software controlled digital phase locked loop.

CONCLUDING REMARKS

Simulation results clearly demonstrate that modified version of the software defined phase locked loop overcomes the gain limitation characteristic of a conventional digital phase locked loop. The signal handling capacity of the modified SDPLL is much more than the conventional one.

REFERENCES

[1] B. N. Biswas, "New software controlled digital phase locked loop", Electronics Letters, vol. 25, no. 9, pp 1097-1098, 3 August, 1989.

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