Efficient Circuit Configurations for Algorithmic ADCs

Veepsa Bhatia[1], Neeta Pandey[2]

[1]Department of Electronics & Communication Engineering, Bharati Vidyapeeth's College of Engineering, A4, Paschim Vihar, New Delhi-110063, India,

email- veepsa@rediffmail.com

[2] As (1) above, email- n66pandey@rediffmail.com

I. INTRODUCTION:

Algorithmic or Cyclic or Recirculating ADCs have the major and distinct advantage of requiring small chip area and low power. This is because they perform the conversion in a serial manner by making repeated use of a simple circuit. This makes it possible to obtain a much better matching accuracy than in large binary-weighted capacitor arrays. The main disadvantage of these ADCs is that they have relatively long conversion cycles, primarily because of their serial nature of operation and also because they necessarily use close-loop amplifiers and not just comparators.

II. BASIC ALGORITHMIC ADC:

A simplified block schematic of the ADC is presented in Fig.1. It consists of an analog arithmetic unit, a sample and hold circuit, a voltage comparator, and a 1-bit memory.

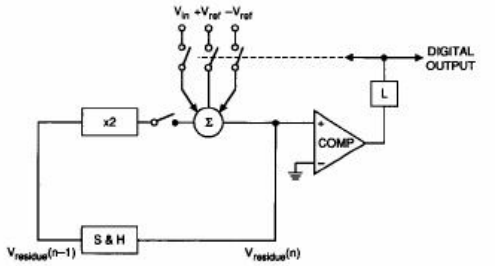

Fig.1. Block Schematic of Conventional algorithmic A/D Converter

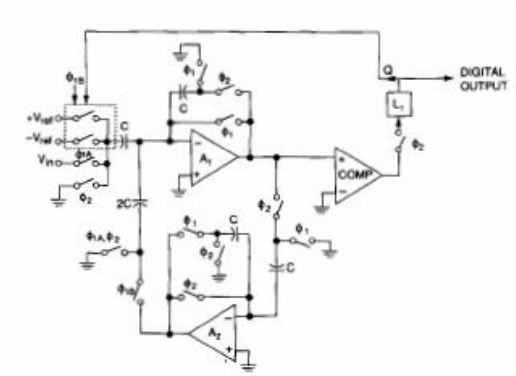

Fig. 2. Circuit Implementation of Fig. 1.

The arithmetic unit is capable of multiplying an analog voltage by a factor of two, as well as adding 1 to it or subtracting from it a reference voltage. In the first step, the arithmetic unit simply samples the input and produces an output equal to V_{in}, which is then compared with zero to decide the MSB. The result of the decision is stored in the 1-bit memory, which is essentially a latch. Simultaneously the output of the arithmetic unit is sampled by the Sample and Hold (S/H) circuit. In the second step, the S/H presents the residue from the first step (equal to V_{in}) to the input of the arithmetic unit, which multiplies it by two and also adds or subtracts V_{ref}, on the value of MSB. This results in a new residue $2V_{in} \pm V_{ref}$, which is then compared with zero to determine the next bit. The process is repeated, once for every bit. In general, the nth step consists of multiplying the residue from the (n-1)th step by two, developing a new residue $V_{residue}(n) = 2\ V_{residue}(n-1) \pm V_{ref}$, and then comparing the new residue with zero to decide the nth bit. The output of the converter is the serial bit stream starting with the MSB. The simplified schematic of the circuit implementation of the configuration of Fig.1 is shown in Fig 2. Here the arithmetic unit is built around the amplifier A1, and the S/H stage is built around A2. This circuit incorporates offset cancellation for the amplifiers and the comparators. $\Phi 1$ and $\Phi 2$ constitute the basic 2-phase non-overlapping clock for the operation of the circuit. The phase $\Phi 1_A$, $\Phi 2_A$, $\Phi 1_B$ and $\Phi 2_B$ are subsets of the basic clocks. The input is sampled during $\Phi 1_A$ and the MSB is encoded during $\Phi 2_A$. This is followed by the serial encoding of the remaining bits. The phases $\Phi 1_B$ are used for sampling the previous residue, whereas the arithmetic operation and the decision making occurs during the phases $\Phi 2_B$.

III. A MODIFIED CONFIGURATION WITH HIGHER THROUGHPUT

The basic configuration needs two clock phases for each bit. The basic reason for this is that it uses a single arithmetic unit sequentially. A modified configuration is shown in Fig.3. Here there are two arithmetic units AU1 and AU2, which operate in tandem. During $\Phi 1_A$, the input is sampled by AU1. Simultaneously, AU2 could be performing arithmetic operations for encoding the last bit of the previous conversion cycle. During $\Phi 2_A$, AU1 is used to encode the first bit of the present sample and the result is stored in L2. This is followed by the sequential encoding of the remaining bits as follows. During the phases $\Phi 1_B$, the arithmetic unit AU2 performs the arithmetic operation under the control of the previous bit stored in L2. The result of the arithmetic operation is applied to the comparator to decide the present bit, which is then latched in L1. Simultaneously, AU1 acts as a sampling circuit to sample the output of AU2. During the phases $\Phi 2_B$, AU1 performs the arithmetic operation on the residue from the previous phase, under the control of the previous bit stored in L1. The output of AU1 is then applied to the comparator to determine the bit, which is then stored in the latch L2.Simultaneoulsy, AU2 acts as a sampling circuit capturing the new residue. Thus, this circuit performs one bit conversion during every clock phase, which means that it has double the throughput of the basic configuration. The digital bits appear alternately at the outputs of latches L1 and L2, starting with MSB, and can be combined to form a single serial word or can be converted in parallel output form.

A. Single amplifier implementation

Fig. 3. can be modified by using a single amplifier between the two arithmetic units. A problem in doing that is the offset cancellation of the amplifiers and the comparators. In Fig. 2, the offset cancellation is achieved by sampling the offsets on the input sampling capacitors. This method needs the amplifiers and the comparators to be connected in unity gain feedback at the time of offset sampling. This is feasible in circuit of Fig.2 because it uses two clock phases for each step. But this scheme cannot be applied to Fig.3 because of its continuous nature of operation. This problem can be overcome by using an auxiliary input to store the offset error, as illustrated in Fig.4. To sample the offset, the main inputs are grounded while the output is fed back to the auxiliary input. The output of the amplifier now equals the total offset from the main path as well as the auxiliary path, both being referred to the auxiliary input. At the end of this phase Φ_{AZ}, the output is disconnected from the auxiliary input, but the input referred amplifier offset error is stored on C_{os}. During the normal operation, the amplifier offset is effectively cancelled by the voltage presented to the auxiliary input. Once the offset error is sampled and held on C_{os}, the amplifier can be used continuously over long periods (several milliseconds) before needing another offset sampling. The extra area needed for incorporating this function is very small. This scheme can be applied to fully differential amplifiers as well.

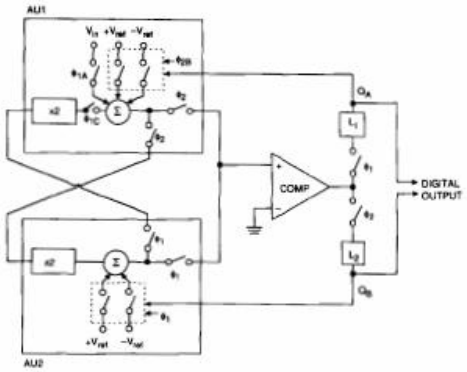

Fig. 3. Alternative Configuration of ADC

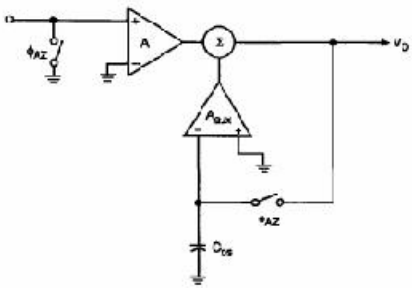

Fig. 4. Offset Compensation Scheme

Using the above offset cancellation technique, we can realize the two arithmetic units in Fig.3 with a single amplifier as shown in Fig. 5. A fully differential circuit is shown here. Comparing the circuits of Fig.2 and Fig.5, the later has several advantages. Firstly, the fact that it uses half the number of amplifiers directly translates into savings in area and power. Secondly, it delivers twice the throughput, meaning that for a given conversion rate, the time available for each multiply-by-2 operation is twice that in circuit of Fig.2, resulting in further saving in power. This advantage is partly offset by the fact that the amplifier in Fig.5 sees a larger capacitive load (about 1.5 times) than the corresponding amplifier in Fig.2. However, the overall power required by the amplifier in Fig.5 is still smaller than its counterpart in Fig. 2. Another factor

that helps in speed and power is that, due to longer time duration, each clock phase, the percentage time lost in generating non-overlapping clocks is smaller in the circuit of Fig.5 than in circuit of Fig.2.

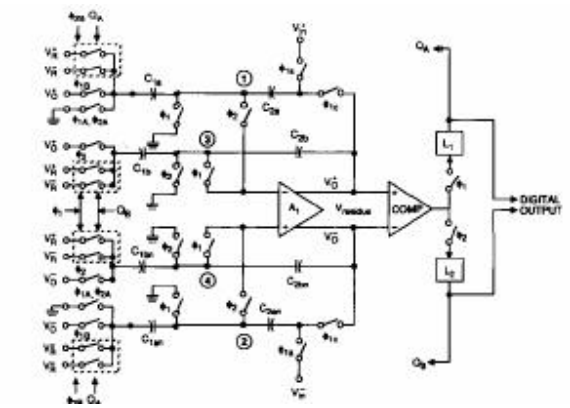

Fig. 5. An ADC using single amplifier

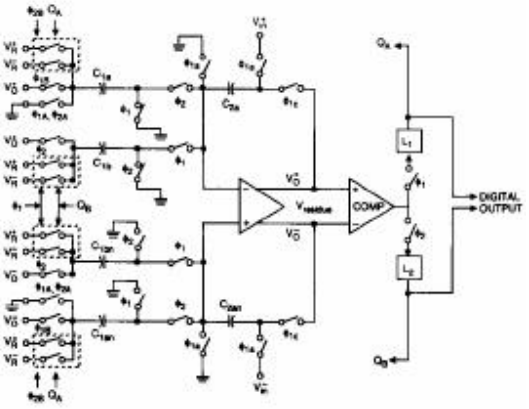

Fig. 6. Further simplification of Fig. 5.

B. Further Simplification

Yet another simplification can be achieved by taking advantage of the fact that for most of the time the capacitor pairs C_{2a}, C_{2an} and C_{2b}, C_{2bn} in Fig.5 are connected either between the amplifier output and the ground or between the amplifier output and the virtual ground (amplifier summing node). Thus, we can replace these two capacitor pairs by a single capacitor pair as shown in Fig.6. Here the input is first sampled onto the capacitors C_{2a}, C_{2an}. For the rest of the conversion cycle, these two capacitors are left continuously connected in the feedback path of the amplifier. The circuit configuration during the odd and even phases would be very similar to those shown in Fig.5, the only difference being the absence of C_{2b}, C_{2bn}. The residue is continuously held on C_{2a}, C_{2an}.During every phase $V_{residue}$ is modified by adding it to quantity $V_{residue} \pm V_{ref}$, depending on the previous decision.

The circuit of Fig.6 is simpler than that of Fig.5 and the capacitive loads on the amplifier are reduced, resulting in higher speed/low power. There are however, certain disadvantages also. Firstly, we need an exclusive phase for sampling the inputs on C_{2a}, C_{2an}. In contrast with the circuit of Fig.5, the input sampling operation can overlap with the last bit of conversion for the previous sample. Another significant advantage of circuit of Fig.5 is that it only needs matched capacitor pairs rather than three matched capacitors. Thirdly, the switches that are adjacent to the amplifier summing nodes in Fig.5 are required to charge only the small input capacitances of the amplifiers and can be made small. This helps to reduce the coupling of power supply though the gate driver of these switches.

C. Clock-feedthrough considerations

Although a simple two-phase clock is assumed in the above description, practical implementations would use modified clocking schemes. This basically involves opening of the switches adjacent to the amplifier summing nodes a little earlier than the other switches in the circuit. This eliminates the signal dependent clock-feedthrough to a first order. Also, the use of fully differential topology offers a first order cancellation of the signal-independent feed-through as well, leaving only a small error due to the mismatches between the two halves of the differential circuit. Fig.7 shows one particularly simple scheme applied to Fig.5. There are a total of five switches associated with these nodes as against four in Fig.5. Of these, only one switch acts as a primary switch providing a charging path for the differential signals. This switch has to be large enough to meet the settling time requirements of the circuit. On the other hand, the two switches from 1 and 2 to ground can be small because they are required only to only make up for any changes in the common mode voltage. Similarly, the two switches from 1 and 2 to amplifier can be small because they don't carry any significant current. The main contributor to the charge feedthrough here would be the large switch between 1 and 2. In the circuit of Fig.5, the switches from 1 and 2 to ground have to provide the charging paths for differential as well as common mode signals. To achieve a desired time constant, the switch between nodes 1 and 2 in Fig.7 needs to be only half as big as the two switches that perform its function in Fig.5. Thus, the switch feedthrough is reduced by a factor of about two by using the scheme of Fig.7.

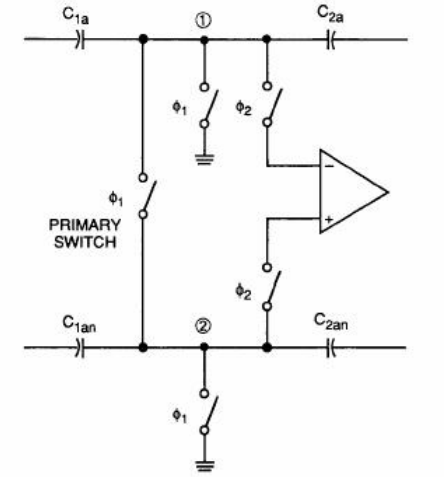

Fig. 7. Scheme to reduce switch feedthrough

IV. CONCLUSION

Several efficient circuit configurations for algorithmic ADCs have been discussed. By using two analog arithmetic units working in tandem, these circuits perform one-bit of conversion in each clock phase, which is the maximum possible throughput achievable from a recirculating architecture. Further by exploiting an offset cancellation method that does not need the amplifier offsets to be sampled once in every clock cycle, single amplifier is time-shared between the two arithmetic units, resulting in a large savings in area and power.

References

1. R.H. McCharles, V.A. Saletore, W.C. Black and D.A. Hodges, “An algorithmic analog-to-digital converter” Proc. Int. Solid State circuits Conf., Feb 1977.
2. H. Ohara, H.X. Ngo, M.J. Armstrong, C.F. Rahim and P.R. Gray, “A CMOS programmable self-calibrating 13-bit eight channel data acquisition peripheral”, IEEE J. Solid State Circuits, vol. SC-22. pp. 930-938, Dec. 1987.
3. C.C. Lee, “A new switched-capacitor realization for cyclic analog-to-digital converter” Proc. Int. Conf on circuits & systems. May 1983.
4. P.W. Li, M.J. Chin, P.R. Gray, and R. Castello,”A ratio-independent algorithmic analog-to-digital conversion technique”, IEEE J. Solid State Circuits, vol. SC-19. pp. 828-836, Dec. 1984.
5. C.C. Shih and P.R. Gray, “Reference refreshing cyclic analog-to-digital and digital-to-analog converters”, IEEE J. Solid State Circuits, vol. SC-21. pp. 544-554, Dec. 1986.
6. H. Onodera, T. Tateishsi, and K. Tamaru, “A cyclic A/D converter that does not require ratio-matched components” IEEE J. Solid State Circuits, vol. SC-23. pp. 152-158, Feb. 1988.
7. B. Ginetti, P.G.A.Jespers and A. Vandemeulebroecks, “A CMOS 13-b cyclic RSD A/D Converter”, IEEE J. Solid State Circuits, vol. SC-27. pp. 957-965, July. 1992.
8. G. Jusuf, P.R. Gray and A.L. Sangiovanni-Vincentilli, “CADICS- Cyclic Analog-to-Digital converter synthesis” Proc. IEEE Int. Conf. On Computer aided design, pp. 286-289, Nov. 1990.
9. K. Nagaraja, “Algorithmic A/D converters”, AT&T Bell Lab. Internal record, Mar. 1991.
10. M. Degrauwe, E. Vittoz, and I. Verbauwhede, “A micropower CMOS instrumentation amplifier”, IEEE J. Solid State Circuits, vol. SC-20. pp. 805-807, June. 1985.
11. B. Ginetti and P.G.A. Jespers, “A 1.5 Ms/s 8-bit pipelined RSD A/D converter”, ESSCIRC Dig. Tech. Papers, pp.137-140, Sept. 1990.
12. K.L. Lee and R.G. Meyer, “Low distortion switched-capacitor circuit design”, IEEE J. Solid State Circuits, vol. SC-20. pp. 1103-1113, Dec. 1985.
13. Veepsa Bhatia, Neeta Pandey, H.M. Rai, “Improving signal processing with ADCs using current mode approach”, National Conference, SLIET-2003, published in proceedings, 2003.
14. Veepsa Bhatia, Neeta Pandey, “Improving signal processing in ADCs”, National Conference On VLSI design and Technology, Bharati Vidyapeeth’s College of Engineering, pp. 50-54 April 2004.