# A MODIFIED TECHNIQUE OF DIRECT DIGITAL FREQUENCY SYNTHESIS USING MULTI FEEDBACK RING OSCILLATOR

**M K Mandal**[(1)] **& B C Sarkar**[(2)]

*[(1)]Department of Physics, National Institute of Technology, Durgapur – 713209, West Bengal, India,*
*E-mail: nitmkm@yahoo.co.in*
*[(2)]Department of Physics, Burdwan University, Burdwan – 713104, West Bengal, India,*
*E-mail: vishbdn@vsnl.net*

## ABSTRACT

Direct digital frequency synthesizer based on accumulators and phase registers, normally use fixed period clock signals. This results in synthesized signals having instantaneously varying time period. A technique of time period modification of the clock signal is proposed here to synthesized fixed period signal. The proposed technique is verified via simulation and hardware experiment.

## INTRODUCTION

Frequency synthesizers are important building blocks of communication systems. Modern wireless communication systems demand frequency synthesizers of high resolution and fast frequency switching speed. The direct digital frequency synthesizers (DDFSs) [1] are able to provide fine step size and required first frequency switching because they have no feedback loop. The disadvantage of the DDFS is large power consumption due to the presences of ROM look-up table in the synthesizer circuit. Therefore the efforts have been made to reduce the ROM size or to eliminate it from FS [2] circuit without degrading the performance of the synthesizer. This paper presents accumulator and phase resister based FS [3], where the most significant bit (MSB) of the phase register gives the synthesized output signal. Conventionally, applying fixed period clock signal at the phase resister, one get the synthesized signal of instantaneously varying time period. To get fixed period synthesized signal we have been used suitable phase modulated clock signal at the clock input of the phase resister.

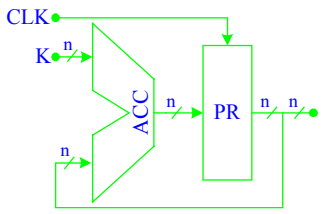


Fig. 1. Block diagram of the conventional DDFS

A phase accumulator-based frequency divider, shown in Fig.-1, is often used in conventional direct digital frequency synthesizer (DDFS) circuits [4]. An $n$-bit accumulator adds with its output stored in an n-bit phase register (PR) with a binary data $k$ (frequency control word) once in every $T_c$ time. $T_c$ is the period of the shifting clock signal applied to the PR. The period of the synthesized output signal taken from the maximum significant bit (MSB) position of the PR will be, on an average,

$$T_r = (2^n/k)T_c \,. \qquad (1)$$

The value of $k$ should be less than $2^{n-1}$ in practice. If $c$ represents the integral part of $(2^n/k)$, then $T_r$ will be between $cT_c$ to $(c+1)T_c$. If the system starts from a reset condition of the PR and $k$ is a number, which can not be represented in the form, $2^t$, where $t$ is positive integer less than $(n-1)$, the content of the PR will be $r$ when the accumulator overflows (i.e, $C_{out}$ is obtained). In this situation one can write

$$(c+1)k = 2^n + r \qquad (2)$$

The synthesized signal is a train of rectangular wave whose period fluctuates between two values $cT_c$ and $(c+1)T_c$ and out of $k$ cycles of the output, $r$ cycles will have a period $cT_c$ while the rest $(k-r)$ cycles will be of period $(c+1)T_c$ . The period of the output signal ($T_r$) is a weighted average of $cT_c$ and $(c+1)T_c$.

$$T_r = [rcT_c + (k-r)(c+1)T_c\,]/k \qquad (3)$$

Thus the synthesized signal would contain a good number of spurious components about an average frequency signal $f_r$, where $f_r$ is related to clock frequency $f_c$ as,

$$f_r = (k/2^n)f_c \,. \qquad (4)$$

The aim of the present work is to modify the circuit in such a way that the output rectangular pulse train can have a fixed period $xT_c$ where $x\ (=2^n/k)$ is a number having integral and fractional parts.

## PROPOSED PERIOD CONTROL ALGORITHM

To synthesized fixed period signal, one clock period, out of each group of $(c+1)$ periods, should have to be adequately shortened. The amount of period reduction can be estimated from the content of the PR, $r$, when the accumulator overflows releasing a "carry out" pulse. The frequency control data to the accumulator being $k$, the period reduction of one clock period ($T_c$ ) should be $(r/k)T_c$ . The intuitive argument of this statement is as follows. If one starts counting time from the reset condition of the accumulator output (also of the PR), the overflow condition occurs when the sum value becomes equal to or more than $2^n$ and a new cycle of the synthesized signal starts. Thus the number $2^n$ is related to the total phase angle ($\phi$) of a complete period, i.e. $2\pi$ and the accumulator control word $k$ is equivalent to a phase angle increment ($\Delta\phi$) of amount ($2\pi k/2^n$). Now, a phase increment of amount $\Delta\phi$ takes place in $T_c$ time, so, when the PR content is $r$, it can be concluded that the phase angle has already increased by an amount ($2\pi r/2^n$). This means the output signal has advanced by an amount of time $(r/k)T_c$ at the beginning of a new cycle. So, to nullify this increase of the PR content or in other words to counter balance the time increment, following steps should be taken: (i) One period of clock signal in every $(c+1)$ periods should be reduced by an amount $(r/k)T_c$. (ii) The content of the PR should be made zero in order to get the overflow condition of the accumulator at the $(c+1)$th period of the clock signal. This will ensure the overflow of the accumulator to occur once in a time interval of $(2^n/k)T_c$ i.e $xT_c$ and the synthesized output waveform would be of fixed period. This will ensure the spectral purity of the synthesized output.

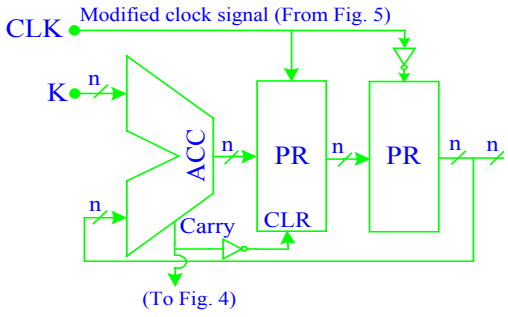



Fig. 2. Block diagram of the proposed DDFS

## HARDWARE STRATEGY

The fixed period synthesizer circuit has been designed using a modified accumulator based frequency divider (Fig. 2) and a multiphase ring oscillator used as the basic clock signal generator. The multiphase ring oscillator can be designed using a finite number of inverters connected in a closed loop chain as shown in Fig. 3(a). The number of different phase

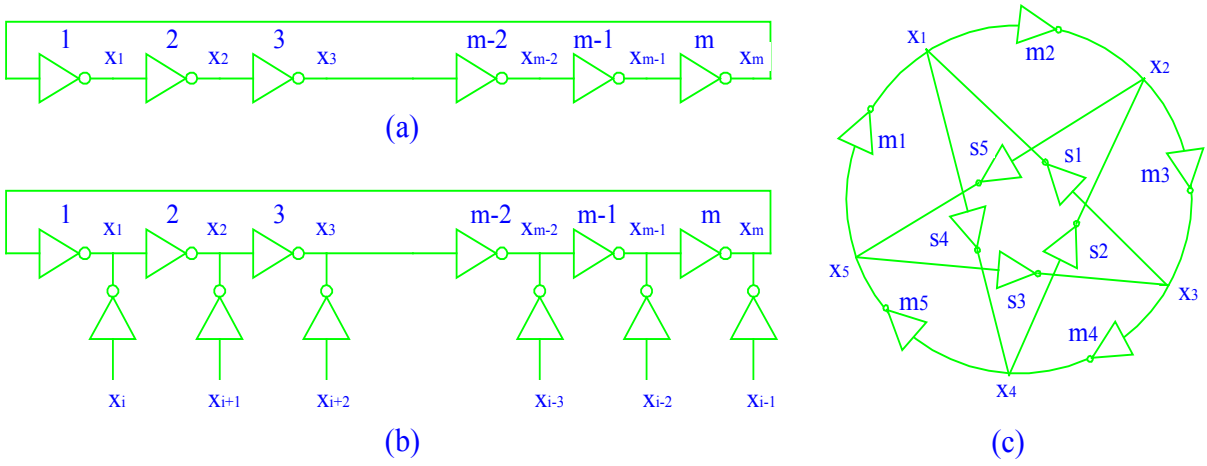



Fig. 3. Ring oscillator: (a) conventional ring oscillator without sub feed back loop, (b) modified ring oscillator with sub feed back loop, (c) Five stages ring oscillator with sub feed back index $b$ =3.

shifted outputs of the RO is same as the number of inverters used in the ring structure. To increase the number of different phase shifted outputs of the RO the length of it will be more, i.e., the number of the inverters used in the ring structure will be more, which leads to decrease the oscillation frequency (speed of operation) of the RO. To solve this conflict between speed and multiphase output, several techniques have been reported in the literature [5-6]. In this work we have used a multi feed back ring oscillator [6] to generate clock signal. Multi feed back ring structure consists of two types of inverter chain: one is long chain, i.e., slow path and another is short chain, i.e., first path. Here the number of phase shifted outputs is equal to the number of inverters in the short chain. This type of ring oscillator is useful for not only in the view of multiphase outputs but also for high speed operation. Fig. 3(b) shows a $m$ stages single ended inverter based multi feedback ring topology with sub feedback index $b$ which is an integer in the range $2 \le b < m$. To understand this ring topology, we consider a $m = 5$ stages RO with feedback index $b = 3$ as shown in Fig. 3(c). This ring structure consists of a slow loop containing five inverters and a five sub feedback fast loops containing three inverters. Therefore the delay of stages is the weighted sum of the delay through the slow path and first path. For example, the delay from node $m_1$ to node $m_2$ is the weighted sum of the slow path delay ($m_2 \rightarrow m_3 \rightarrow m_4$) and the first path delay $s_4$. The phase relationship between inverter stages remains unchanged due to the symmetrical structure. In the hardware experiment we have used 17 stages RO with $b = 15$.The period of this oscillator is discretely modulated with the help of a multiplexer which selects one properly phase advanced output of the ring oscillator. Therefore the MUX serves as the purpose of a phase shifter. The phase shift between the previous and the present output signal of the MUX depends on its digital controlled word. A specially designed circuit (Fig. 4) provides the suitable selection word for the multiplexer to satisfy the design algorithm. A $m$ stages single ended inverter based RO with sub feedback index $b$ can provide $b$

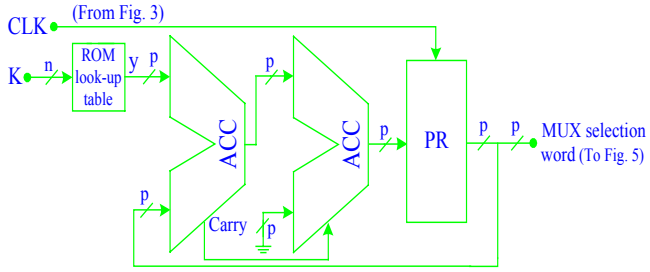



Fig. 4. MUX selection word generating digital circuit

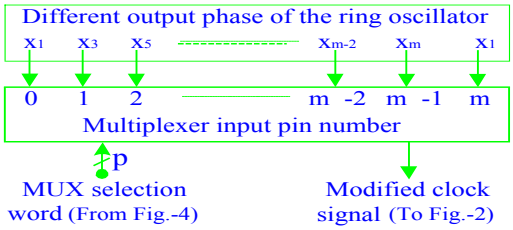



Fig. 5. Connection between the different phase shifted outputs of the ring oscillator and the input terminals of the multiplexer.

square wave signals of equal time period but differing in phase; the phase difference between two properly chosen signals is ($2\pi i/b$) where $i$ is an integer in the range 1 to ($b$-1). Any one of these $b$ signals can be selected with the help of a suitable multiplexer. The input of the MUX is so chosen that the output of the MUX for two consecutive selection words differ by a phase ($2\pi/b$). This is realised by applying the alternate outputs of the RO to the MUX inputs in a proper sequence. First the outputs of the odd numbered inverters (1,3,5 ...) are applied to the consecutive inputs of the MUX (0,1,2,3, …) and then the outputs of the even numbered inverters (2,4,6, …) of the RO are applied to the MUX input terminals (Fig. 5). The last input (15) of the MUX is same to its first input (0). The multiplexer selection word (SW) is of $p$ bits ( $p \le \log_2^b$ ) and it is chosen depending on the value of the PR content r at the instant when the accumulator overflows. The design algorithm demands that, at that instant, the basic clock period should be reduced by $(r/k)T_c$ which is equivalent to a phase change ($2\pi r/k$). Since a change of phase by ($2\pi/b$) is obtained by changing the selection word by unity, the MUX selection word should be changed by $y$ where $y = b(r/k)$ to get required phase change. A logic circuit based on two full adders (FAs) and a shift register (SR) determines the MUX selection word in real time adding y with previous control word. If the first FA overflows, the actual control word is obtained by adding one with the sum output of the first FA with the help of the second FA as shown in Fig. 4. For a particular design, with given values of $n$ and b, $r$ is fixed for a given $k$; and so $y$ is known. Thus a ROM look-up table can be used to get $y$ for a given k.

## EXPERIMENTAL RESULTS

Using commercially available TTL building blocks the hardware algorithm has been tested in an experiment. For simplicity and without the loss of generality, the following values have been taken in the experiment: 4-bit FAs, 4-bit SRs, 16-inputs to 1-output MUX, 4-bit MUX control ward. Fig. 6 shows fifteen different phase shifted outputs of an RO in proper sequence and these are the consecutive inputs (from 0 to 14) of a 16 inputs to 1 output MUX. The inputs 0 and 15 of the MUX are same. Experiment has been performed for different values of k and the spectrum of the synthesized

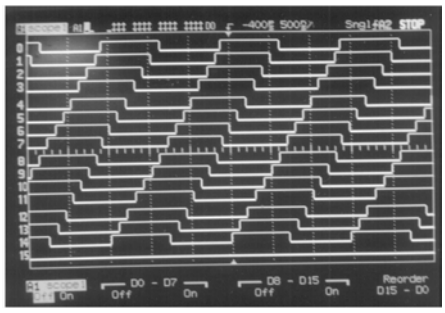


Fig. 6. Different phase shifted signal of the ring oscillator in a proper sequence.

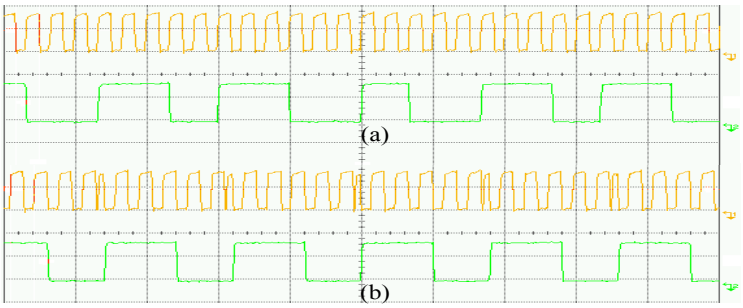
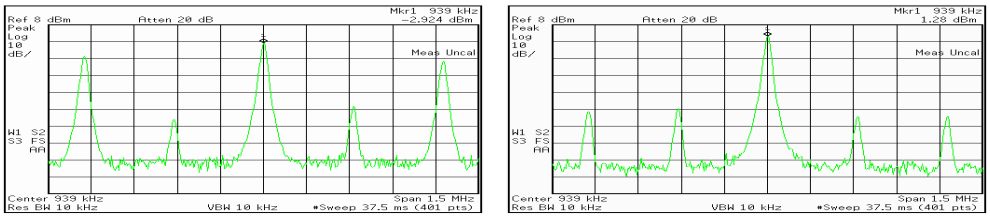



Fig. 7. Time domain view of the clock signal and synthesized output: (a) using conventional DDFS (b) using proposed DDFS. Horizontal axis: 0.5μs/div. Vertical axis: 2V/div.

signal with and without modification has been obtained. Fig. 7(a) shows the time domain tracings of the clock signal used and the synthesized signal for a conventional DDFS when the value of k = 3. Here the time period of the clock is fixed and the time period of the synthesized signal is changing. The clock and synthesized signals for the modified system is given in Fig. 7(b) which shows require modified clock signal and fixed period synthesized signal. The shortened time period of one cycle in every 6 cycles is evident from the figure and the fixed period output signal is also evident. Fig. 8(a) shows the spectrum of the synthesized output from a conventional DDFS whereas Fig. 8(b) depicts the same form the modified system. The reduced power of the side band components gives the evidence of improved performance of the modified systems. When the frequency control word changes at a rate of 8μs between two values 0011 and 0101 then the synthesized signal switches between the values 939KHz and 1565KHz respectively.




(a) (b)

Fig. 8. Spectrum of the synthesized signals (a) using conventional DDFS (b) using proposed DDFS. ($f_c$ = 5.008MHz, $n$ = 4, $k$ = 3)

## CONCLUTION

The success of the proposed algorithm lies on the ability of the design of a circuit capable of reducing a clock period by proper amount. The digital technique proposed here heavily depend on the multistage ring oscillator design and the value of $m$ restricts the maximum value of $k$, which can be used. Even though the experiment has been done at the lower end of the RF spectrum, using high frequency building blocks, the system can be implemented at much higher frequencies.

## REFERENCES


[1] A. N. Mohieldin, A. A. Emira, and E. Sancher-Sinencio, "A 100MHz 8mW ROM less quadrature direct digital frequency synthesizer," IEEE J. of Solid State Circuits, vol. 37, pp. 1235-1243, October 2002.

[2] S. Mertezapour, and E. K. F. Lee, "Design of low power ROM-less direct digital frequency synthesizer using non-linear DAC," IEEE J. of Solid State Circuits, vol. 34, pp. 1350-1359, October 1999.

[3] A. Madisetti, A. Y. Kwentus, and A. N. Willson, "A 100MHz, 16-b, direct digital frequency synthesizer with a 100-dbc spurious free dynamic range," IEEE J. Solid State Circuits, vol. 34, pp. 1034-1043, August 1999.

[4] Kropa V F, Direct Digital frequency synthesizer, IEEE Press, 1998.

[5] S. J. Lee, B. Kim, and K. Lee, "A novel high speed ring oscillator for multiphase clock generation using negative skewed delay scheme," IEEE J. of Solid State Circuits, vol. 32, pp. 289-291, February 1997.

[6] L. Sun, and T. A. Kwasniewski, "A 1.25-GHz 0.35-μm monolithic CMOS PLL based on a multiphase ring oscillator," IEEE J. of Solid State Circuits, vol. 36, pp. 910-916, June 2001.