HARDWARE IMPLEMENTATION OF SMART ANTENNA SYSTEMS FOR HIGH SPEED WIRELESS COMMUNICATION

Hiroyuki ARAI[(1)], **Koichi ICHIGE**[(2)]

[(1)] ***Department of Electrical and Computer Engineering, Yokohama National University 79-5 Tokiwadai, Hodogaya-ku, Yokohama 240-8501, Japan, E-mail: arai@ynu.ac.jp***
[(2)] ***As (1) above, but E-mail: koichi@ynu.ac.jp***

ABSTRACT

This paper presents some hardware implementation results of DOA (Direction Of Arrival) estimator and beamformer developed by our smart antenna project for high speed wireless data transmission. The present system employs smart antenna, FPGA-based digital signal processor and several analog & digital techniques in RF, IF and digital processing, and can estimate DOAs and do beamforming at very high speed and high accuracy. Performance of the present system is evaluated through some experiments.

1 INTRODUCTION

Smart antenna system which enables ultra high speed DOA (Direction Of Arrival) estimation and beamforming at reasonable cost is desired for high speed wireless data transmission. Beyond IMT-2000 mobile communication system, ultra high speed wireless data transmission more than 100 Mbps will be expected in the near future. It is needed to develop an efficient smart antenna system which searches location of mobile terminal and directs a sharp beam to the target direction. Adaptive antenna algorithms can be found in many references, however, there exists small number of literatures about hardware architecture for such systems. Smart antenna is an adaptive antenna system involving spatiotemporal baseband signal processing. Before the baseband processing, well-calibrated multichannel receiver/transmitter and high resolution AD/DA converters are required.

In this paper, some example hardware implementation results of DOA estimator and beamformer are presented. The target system is DBF (Digital BeamForming) antenna based on DOA estimation to find an optimum transmitting antenna radiation pattern. We first introduce the whole system configuration with significant digital and IF sampling techniques. Then we develop Unitary MUSIC (MUltiple SIgnal Classification) Processor (UMP) toward very high speed DOA estimation. Also we present a real-time beamforming system using UMP and see its performance.

2 SYSTEM CONFIGURATION

In this section, the whole system configuration is briefly described and then some significant modules are shown [1].

The present hardware implementation of smart antenna system consists of ULA (Uniform Linear antenna Array) with half-wavelength interval each, multichannel calibrated transceiver, AD/DA converters and FPGA-based digital processing unit together with optimum DOA estimation and beamforming algorithms. Received signals are downconverted by multichannel transceiver, and then digitized by AD converter. Digital processor estimates DOAs and forms a beam in order to receive target signal while eliminating interferences.

AD/DA conversion is especially a significant module in the whole system architecture. The traditional super-heterodyne receiver in Fig. 1 becomes larger scale as the number of antenna elements gets bigger, and the nonlinearity & imperfection of analog devices between channel branches make harmful effects. Therefore, such traditional analog architecture is replaced by low-IF sampling downconversion module shown in Fig. 2 [2]. This architecture directly digitizes received signals at IF stage, and then complex digital signals are demodulated. Single high speed AD converter corresponding to high frequency input signal is required in each channel, hence low-IF sampling is attractive architecture for multiple channel system.

Table 1 shows example specifications of FPGA-based digital processing unit. In the receiving part, filtered and amplified RF signals are downconverted to low-IF by super-heterodyne receiver. Reciprocally, digital baseband signals in the transmitting part are modulated and upconverted by DUC (Digital UpConverter) on FPGAs, and converted to analog low-IF signals by DACs. After a few stages of upconversion to RF, the transmitting signals are emitted from antenna array.

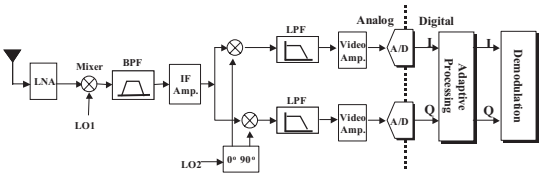

Figure 1: Baseband Sampling Rx Architecture

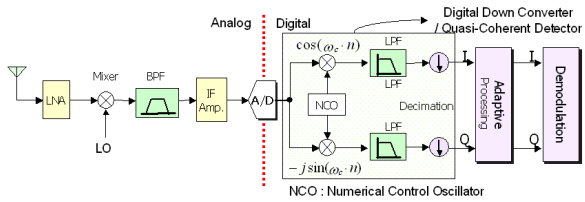

Figure 2: IF Sampling Rx Architecture

Table 1: Specifications of the proposed system

IF freq.	10MHz (Oversampling) 40MHz (Undersampling)	
ADC (Rx)	Channels	Up to 16
	Resolution	12 bits
	Sampling Rates	Up to 40MHz
DAC (Tx)	Channels	Up to 16
	Resolution	14 bits
	Conversion Rates	Up to 160MHz
FPGAs	ALTERA APEX20KC600 (About 600K Gates × 5 = 3M gates)	
CPU	HITACHI SH4	
OS	NetBSD	
User I/F	Ethernet	100BaseT

Table 2: Simulation Parameters

Antennas	8-Element ULA ($\lambda/2$)	
DOA Estimator	16-bit Fixed Point-UMP w/o Spatial Smoothing	
Beamforming	Null-steering Dolph-Chebyshev Beamformer (NDC-BF), SLR=40dB	
Transmitting Signal	$\pi/4$-DQPSK	
Burst Frame Length	136 Symbols (272 bits)	
Incident Waves	User	0°
	Interferers	-20, 15° (In-Beam), -40° (Out-of-Beam)
Channels	AWGN and Rayleigh Fading (AS = 3°, $N_i = 30$)	
Doppler Freq.	0 (Burst Stationary Slow Fading)	
Trials	2000	

3 FAST DOA ESTIMATOR BY UNITARY MUSIC PROCESSOR (UMP)

Unitary MUSIC Processor (UMP), an FPGA-based DOA estimation system based on Unitary MUSIC algorithm is reported in this section [3].

We implement the system on 2 FPGAs (EP20K600, Altera) which had about 1.2 million equivalent gates and 80 Kbytes internal memory block totally. The whole block diagram of the DSP procedures is shown in Fig.3. It is involved in 4 major procedure sections including Correlation Matrix Section, EVD Section, FFT Section and LM Detection Section. The bit precision of every section is also shown in this figure. Here we assume that the exact number of waves were predetermined and known in advance from any other process.

In our evaluation testbed as shown in Fig.4, RF signals are downconverted to IF signals centered at 10MHz in analog DC receiver, and then digitized by ADCs at the rates of 40MSPS. The 4 times oversampled IF signals are digitally downconverted once again to complex baseband and then L-times downsampled, where L is an appropriate integer. The FPGAs perform the digital signal processing of the unitary MUSIC algorithm.

Figure 5 shows the hardware level simulation results, where the squared, diamonded and triangled line at 0, 30 and 60 degrees respectively were processed by UMP, and the circled line was obtained by an offline PC with 64-bit floating-point operation. This measurement included 1000 trials(bursts) data of 32 snapshots. The source wave was a CW signal. In this result, it is clear that the estimation accuracy is below 2 degree if the input SNR is greater than 5 dB in the linear region between -30 and $+30$ degrees.

4 UMP-BASED BEAMFORMER FOR ELIMINATING INTEFERENCES

A beamforming system based on UMP is introduced and evaluated in this section [4].

The proposed system consists of a DOA estimator and a beamformer as shown in Fig. 6. The DOAs of the user signal and interferers are estimated and assumed to be classified properly. The beamformer employs equiripple Dolph-Chebyshev beam with sidelobe ratio (SLR) of 40 dB. It steers the mainlobe toward the user direction and totally suppresses the interferers by low sidelobe.

The performance of the proposed system including DOA estimator and DOA-based beamformer is evaluated through computer simulations. Assume that four waves including single user and three interferers (two of them are in-beam interferers) arrived at 8-element half-wavelength ULA. The other detail parameters are given

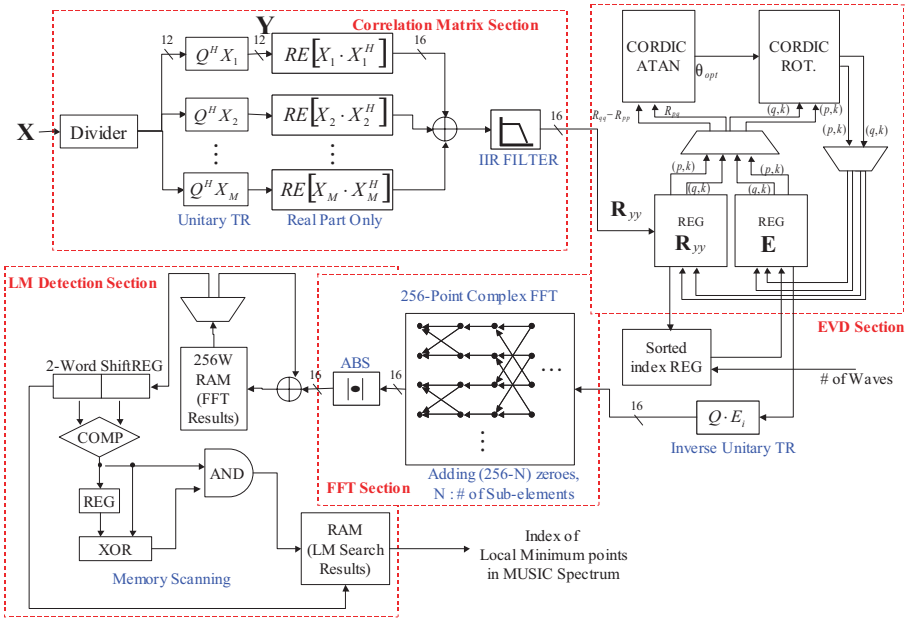

Figure 3: DSP block Diagram

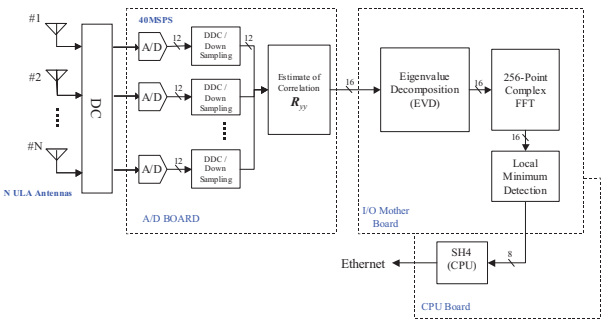

Figure 4: Whole Evaluation System Configuration

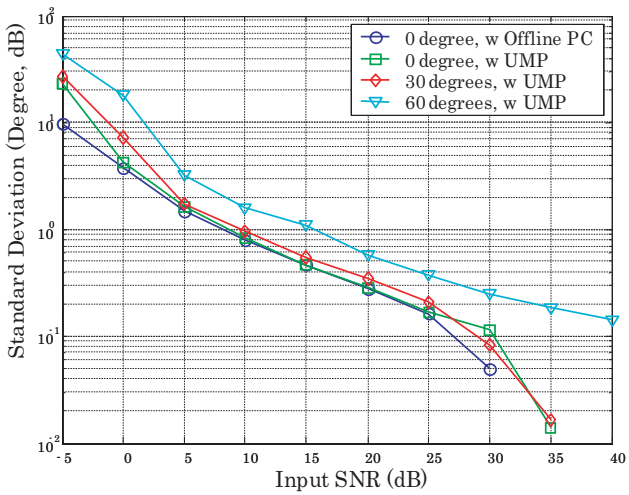

Figure 5: Standard Deviation of Estimated DOA when single wave impinging at 0, 30 and 60 degrees

in Table 2. We also computed the performance of conventional uniform beamformer (Uniform-BF), Dolph-Chebyshev beamformer (DC-BF) and Zero-forcing (ZF) to compare with the proposed system.

Figure 7 shows the typical beampatterns. In AWGN channel, planar wave model with no fading is assumed. However, in Rayleigh fading channel the signal level becomes random variable and the DOA is spread by local scatterers. Thus beamforming with the instantaneous DOA estimation result based on the planar wave assumption leads performance degradation. Figures 8 and 9 illustrate the performance of bit error rates (BER) in AWGN and Rayleigh fading channel. The average INR (Interferer to Noise Ratio) of each interferer was set to 9dB. The number of sources is assumed to be perfectly known in advance. In these results, the proposed system has comparable to ZF technique that known for the optimum beamformer, while the computation load is extremely low for that of ZF.

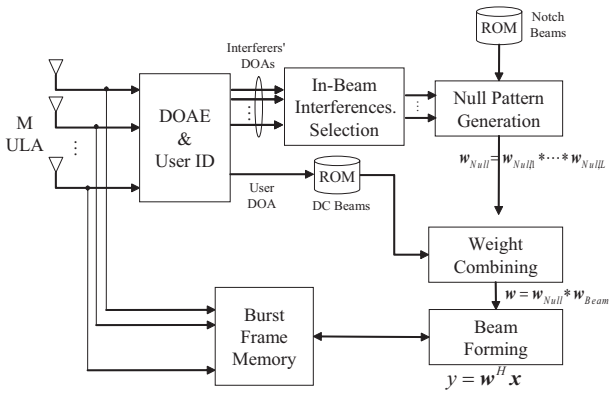

Figure 6: Realtime UMP-Smart Antenna System

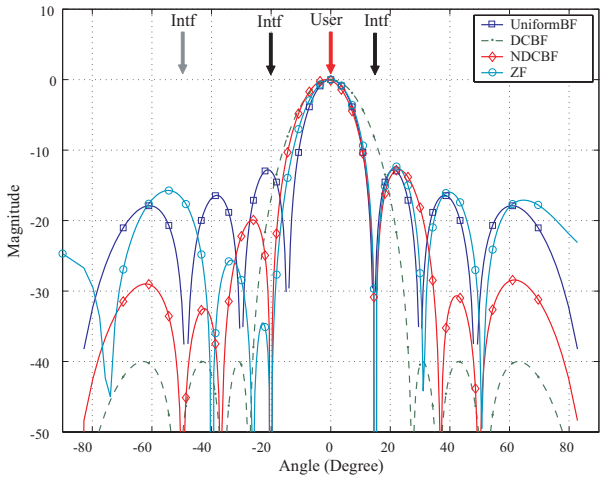

Figure 7: Typical Beampatterns

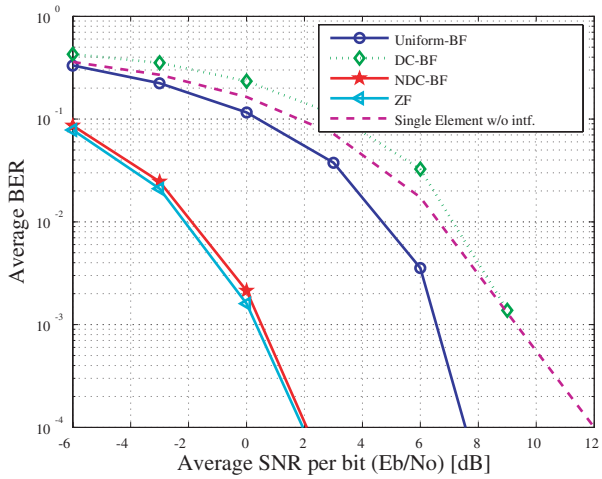

Figure 8: BER Performance (AWGN Channel)

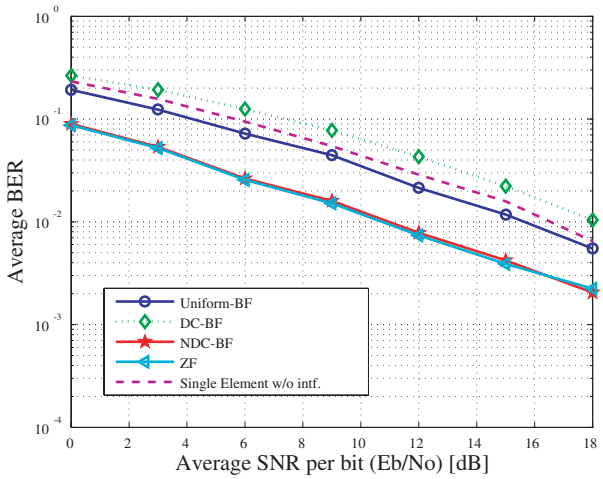

Figure 9: BER Performance (Rayleigh Fading Channel)

5 CONCLUDING REMARKS

Hardware implementation results of DOA estimator and beamformer was presented. The present systems employed smart antenna, FPGA-based digital signal processor and several analog & digital techniques in RF, IF and digital processing. The present system can estimate DOAs and do beamforming at very high speed and high accuracy. Those systems will be used in mobile communication, especially in ultra high speed wireless data transmission.

REFERENCE

[1] H. Arai and M. Kim, "Hardware Design of RF and Digital Units for Smart Antenna System," Proc. Asia-Pacific Microwave Conference (APMC), Seoul, Korea, Oct. 2004.

[2] M. Kim, A. Kiyono, K. Ichige and H. Arai, "Experimental Study of Jitter Effect on Digital Downconversion Receiver with Undersampling Scheme," IEICE Trans. Info. & Syst., vol.E88-D, no.7, p.1430-1436, July 2005.

[3] M. Kim, K. Ichige and H. Arai, "Implementation of FPGA based Fast DOA Estimator using Unitary MUSIC algorithm," Proc. IEEE Vehicular Technology Conference (VTC 2003-fall), Orlando, FL, U.S.A., Oct. 2003.

[4] M. Kim, K. Ichige and H. Arai, "Real-Time Smart Antenna System Incorporating FPGA-Based Fast DOA Estimator," Proc. IEEE Vehicular Technology Conference (VTC 2004-fall), Los Angeles, CA, U.S.A., Sep. 2004.