VARIATION OF THE TRANSPORT PARAMETERS WITH TEMPERATURE AND THEIR ROLE IN MICROSTRIP LINE INTEGRATED JOSEPHSON SERIES ARRAY VOLTAGE STANDARD

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ABSTRACT

In the present paper we will discuss, in brief, some aspects of the fabrication of the trilayer ($Nb/Al_2O_3/Nb$) of the Josephson series array integrated into microstrip line and containing 2000-14000 tunnel junctions. The two fabrication processes (where author has some experience at PTB, Germany) used were namely 'SNEP' (Selective Niobium Etching Process) and 'SAWW' (Self Aligned Whole Wafer). Further we discuss two important issues which were found useful for the performance of the Josephson series arrays in generating stable constant voltage steps namely, the role of (i). Microwave coupling from a source (klystron or a Gunn oscillator) to each junction of the array and (ii). Transport parameters.

INTRODUCTION

Discovery of Josephson effects by Brian Josephson in 1962 had open a new era in the field of superconducting electronics. One of the device is the microstrip line integrated Josephson series array used world over in the 'National Measurement Institute' for the generation of the primary standard of the unit 'volt' with the highest precision. At NPL-India, author has established this measurement facility [1] using the array fabricated by him at PTB, Germany under NPL-PTB Phase - II programme.

In the present paper we will discuss, in brief, some aspects of the fabrication of the trilayer ($Nb/Al_2O_3/Nb$) of the Josephson series array integrated into microstrip line and containing 2000-14000 tunnel junctions. The pros and cons of the two processes (where author has some experience) namely 'SNEP' (Selective Niobium Etching Process) and 'SAWW' (Self Aligned Whole Wafer) will be highlighted.

SELECTIVE NIOBIUM ETCHING PROCESS (SNEP)

PTB, Germany in 1989 has successfully developed its tri-layer ($Nb/Al_2O_3/Nb$) technique integrated into microstripline using the SNEP (Selective Niobium Etching Process) for the fabrication of the series arrays to be used in the development of the new generation Josephson series array voltage standard at 1 V and 10 V levels [2]. The number of junctions in series in the circuits varied from 2000 to 20,000. Author has also fabricated arrays for use at NPL-India under the NPL-PTB co-operation programme using the various fabrication process employed at PTB for making the 1 volt, 10 volt standard arrays and switching circuits [3].

One of the important advantages of the above process in the circuits is that the critical current of the array can be changed even after the fabrication by tempering at various temperatures [4]. The observed effect may be due to the changes in the thickness of the tunnel barriers by the heat treatment.

These arrays were to be used for the establishment of the Josephson voltage standard at National Physical Laboratory (NPL), India but their quality deteriorated and precision measurement could not be done. To avoid the deterioration and the formation of the additional $Nb/Nb_2O_5/InPb$, to some extent, we have deposited a thin layer of Au (approximately 10 to 20 nm) insitu over the sandwich. It was found to be useful, but need more systematic work to optimize and to understand explicitly the behaviour of this thin Au layer. PTB, Germany also found the drawbacks regarding the quality and reproducibility of these circuits especially in the fabrication of 10-Volt arrays. It was found that the pin holes formed in the SiO/SiO_2 window layer used in this technique was responsible in generating the flux traps and in turn results into small current amplitude and unstable steps. Also aging effects like deterioration in dc characteristics and in some cases poor coupling of the rf power was observed resulting in low voltage steps unsuitable for precision measurements. Recently they have improved and modified their fabrication process known as SAWW process.

SELF ALIGNED WHOLE WAFER PROCESS (SAWW)

Mueller et al [5] at PTB have redesigned and developed an improved variation of the self aligned whole wafer process (SAWW) first reported by Blamire et al [6]. This modified process has helped in improving upon the problems mentioned earlier and led to the increase in the yield of the good quality voltage standard at 1 and 10 Volts levels. The results reported in this paper are on the chips fabricated by the author at PTB using this SAWW process.

PRECISION MEASUREMENT

At NPL- India, these chips fabricated by the author using the above mentioned SAWW process are being used for the precision measurement/ calibration and were found to be of good quality especially having large current amplitude and stable steps. Fig. 1(a) shows the dc characteristics of one of the chip fabricated by the author containing 3216 $Nb/Al_2O_3/Nb$ tunnel junctions in series and it reaches circuit's gap voltage. When this chip was irradiated by the microwave frequency at 73 GHz of Gunn oscillator it generates large current amplitudes ($\Delta I = 30\ \mu A$) of the constant voltage steps as shown in Fig. 1(b). The rf power used were found to be less in comparison of the arrays fabricated by the SNEP process and no flux trapping was observed during several thermal cycling.

These constant voltage steps are used for the precision calibration and to provide the traceability in the country, for unit 'volt' using the well-known Josephson voltage equation:

$$\mathbf{V = nf / K_{J\text{-}90}} \qquad \mathbf{(1)}$$

Where $\mathbf{K_{J\text{-}90}}$ **= 483597.9 GHz/V** as international agreed value.

f = frequency and n = 0, ± 1, ± 2, ±3, ----

All measurement has certain degree of uncertainty. The total uncertainty evaluated at 1 volt level, at k=1 is ± 20 nV (it does not include the uncertainty of the noise of the Zener diodes; normally they vary from ±50 to ±100 nV). The uncertainty budget based on the ISO/IEC 17025 guidelines is given in the Table 1.

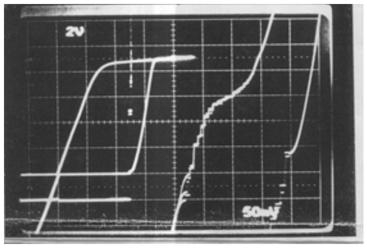
The uncertainty budget for the calibration of the Zener standard diode is as given below.

Table 1: Uncertainty budget

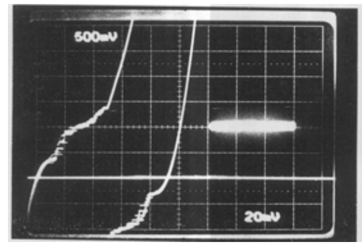
S.No.	Quantity	Probability distribution Type A or B	Uncertainty contribution
1.	Repeatability	Type A	12 nV
2.	Frequency offset	Type B	14.5 nV
3.	Leakage resistance	Type B	3.5 nV
4.	Resolution of DMM	Type B	2.5 nV
5.	Drift during measurement	Type B	4.0 nV

During the precision measurement it was found that the performance of the Josephson series arrays in generating stable constant voltage steps depends on the two issues namely, the role of (i). Microwave coupling from a source (Klystron or a Gunn oscillator) to each junction of the array and (ii). Transport parameters.

In generating constant voltage steps, one of the issues namely microwave coupling from a source (Klystron or a Gunn oscillator) to each junction of the array plays an important role. First of all there should be the optimized impedance matching between the waveguide to the stripline and to the each junction so as to couple the maximum power. Secondly, the maximum step voltage obtained is found to be proportional to √Power as also reported in reference [7].
This in turn depends on the number of the splitted stripline. Less means low power required for generating zero-crossing voltage steps. More means high power requirements and problems of stability etc. associated with it. In collaboration with Y. Sakamoto of ETL, Japan (now NMIJ) we have observed that the even the slight variation of the frequency leads to the large reduction of the zero crossing voltage in chips fabricated by ETL and by the author at PTB (details will be published elsewhere).
The role of the transport parameters such as resistance (R), current – voltage (I-V) characteristic, gap energy (ΔE_g) and critical current (I_c) in the understanding of the arrays is discussed herewith. For this we have carried out experiments and evaluated them in the range from 3 K to the transition temperature (T_c) of niobium and upto room



(a) Left hand side quadrant: I-V characteristics of the array.
Vertical: 2V/div. Horizontal: 50 μA/div.
The overlapping characteristic is at higher resolution to observe any flux trapping.
Vertical : 10 mV/div. Horizontal: 50 μA/div.
Right hand side quadrant: Characteristics when the array is irradiated with microwave at 73 GHz



(b) Left hand side quadrant: Characteristics when the array is irradiated with microwave at 73 GHz
Right hand quadrant: Constant voltage step at
Horizontal: 10 μA/div. $\Delta I = 30\ \mu A$

Fig. 1 DC characteristics of the series array of 3216 $Nb/Al_2O_3/Nb$ tunnel junctions fabricated by SAWW process

temperature. A Si diode is used for measuring the temperature and is directly mounted on the array. The resolution and the drift of the temperature measurement are less than 1 mK. The variation of the resistance as a function of the temperature of the array (as a case study we have taken $Nb/Al_2O_3/Nb$ array containing 3000 tunnel junctions and fabricated using SNEP process) gave the, T_c, of niobium as 8.4 K and for the PbIn used for wiring layer as 6.8 K. The data of the transition suggests that the quality of the film is good. After the measurement of the resistance, the I-V characteristics (Fig. 2) were recorded on the oscilloscope by providing the current from an analogue current source. From these curves the experimental values of (ΔE_g) and critical current (I_c) were obtained and plotted in the Fig. 3(a,b).

Experimental data of Fig. 3(a), when compared with the theoretical values of (2) and Fig. 3(b) when compared with theoretical values of Ambegaokar and Baratoff theory (3) show very good agreement suggesting the good quality of the fabricated array.

$$I_c(T) = \{\pi\, \Delta(T)/2\, R_N\}\tanh(\Delta(T)/2k_BT) \tag{2}$$

$$\Delta(T) \approx 1.74\, \Delta(0)\, \{1-(T/T_c)\}^{1/2} \tag{3}$$

During measurement the quality of the array was reflected, as we found that the array require low microwave power (-6 dB) to generate the constant voltage step with a large value of current amplitude ($\Delta I = 40\ \mu A$) and it was very stable for long time (2 hrs), thus facilitate in the precision measurement and calibration. Similar results were obtained with arrays (fabricated by either SNEP or SAWW process) having experimental (ΔE_g) and (I_c) agreeing with the theoretical values. Thereby the understanding of microwave coupling and transport parameters play a useful role in the establishment of the Josephson series array voltage standard.

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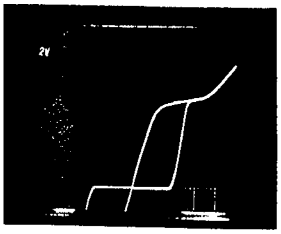
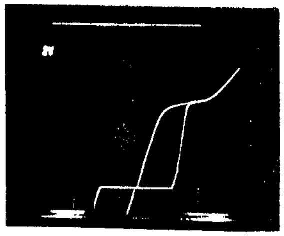
REFERENCES

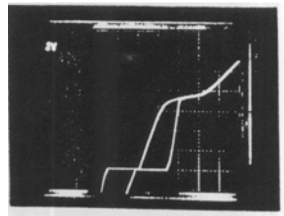
[1] V. N. Ojha and A. K. Gupta, “Josephson series array voltage standard at National Physical Laboratory, India”, *CPEM’98, 6-10 July 1998, Washington D.C.,USA*, Edited by: T.L. Nelson, pp. 558-559, 1998.



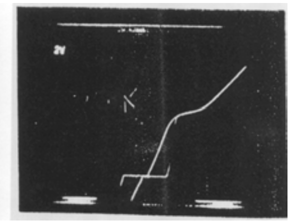
(a). 3.020 K



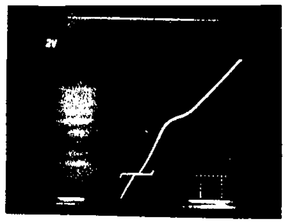
(b). 4.059 K



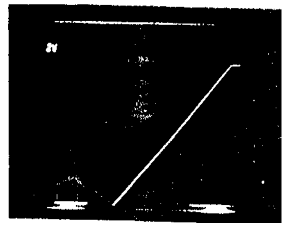
(c). 5.011 K



(d). 6.059 K

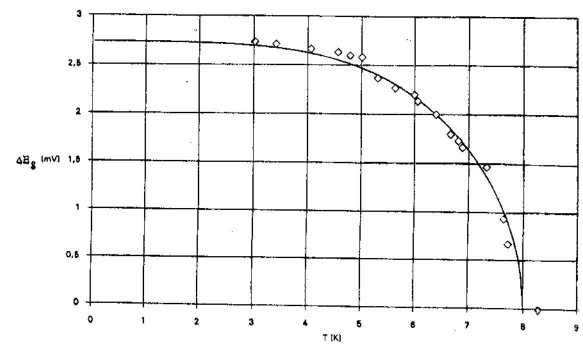


(e). 6.813 K

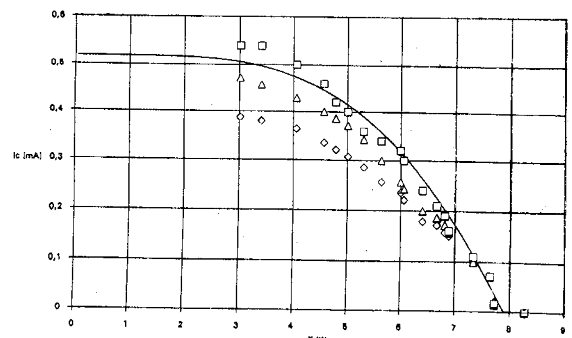


(f). 8.280 K

Fig. 2 I-V characteristic versus temperature as recorded for the array by oscilloscope
Vertical : 2V/div. Horizontal: 200 μA/div.



(a)



(b)

Fig. 3(a) The plot of ΔE_g versus temperature. The solid line is the theoretical curve using BCS approximation.

Fig. 3(b) The plot of I_c versus temperature. The solid line is the theoretical curve using Ambegaokar and Baratoff theory. The experimental values of I_c as measured at the (◊) lowest curve, at the (Δ) middle part and at the (□)upper part of the oscilloscope.

[2] R. Popeal, J. Niemeyer, R. Fromknecht, W. Meier and L. Grimm, “1 V and 10 V seriesarray Josephson voltage standards in Nb/Al2O3/Nb technology”, *J. Appl. Phys*., vol. 68, pp. 4294-4303, Oct., 1990.

[3] V.N. Ojha, R. Popel, J.Niemeyer, L. Grimm, L. and W.Mejer, “Fabrication of Nb/Al2O3/Nb Josephson arrays and the application as voltage standard and switches, in *Weak Superconductivity*, Eds: Benacka, S; Darula, M and Kedro, M, World Scientific, Singapore, pp. 194-202, 1991.

[4] V.N. Ojha, “Low Tc Josephson tunnel junctions and their devices”, *IETE Journal of Research*, vol.45, pp.257-264, May-August 1999.

[5] F. Mueller, R. Popeal, J. Kohlmann, J. Niemeyer, W. Meier, T. Wiemann, L. Grimm, F. W. Duenschede and P. Gutmann, “Optimized 1 V and 10 V Josephson series array”, *IEEE Trans. Instrum. Meas*., vol. 46, pp. 229-232, April 1997.

[6] M.G. Blamire, J.E. Evetts and D.G. Hasko, “A new self aligning process for whole wafer tunnel junction fabrication”, *IEEE Trans. Instrum. Meas*., vol. 25, pp. 1123-1126,1989.

[7] Y. Sakamoto, “Experimental study on millimeter wave attenuation in Josephson junction striplines for voltage standards”, *PTB-Mitteilungen*, Vol. 104, pp. 151-157, 1994.