SCALABLE ARCHITECTURE FOR COMPUTATIONALLY INTENSIVE SOFTWARE RADIO SYSTEMS

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ABSTRACT

The use of software radio technology will predominate the next generation of military radios, such as the Joint Tactical Radio System (JTRS) "Cluster One" being procured by the United States. The use of software radio technology is already widespread in commercial wireless base stations, and is spreading rapidly to mobile terminals. This paper examines military and commercial use cases involving Software Communications Architecture (SCA) "systems of systems" which require computationally dense implementation, in the range of 1–100 giga-operations per second (GOPS), leading to the use of scalable multicomputing, switch fabrics, and real-time, data-parallel CORBA.

INTRODUCTION

Software defined tactical radios are currently being procured by the United States, which complies with a common architecture called the Software Communications Architecture (SCA) [1]. The first of these software radio procurements is called JTRS Cluster One, a family of tactical radios for use in ground vehicles and helicopters, which is in source selection as of this writing. The SCA is undergoing international standardization efforts including:

SCARI: SCA Reference Implementation. This open-source platform specific model (PSM) is based on the SCA 2.2 and CORBA (Fig. 1). SCARI is under development by Canada's Communications Research Centre (CRC), sponsored by Canada's Defense Research Establishment Ottawa (DREO) and the Software Defined Radio Forum (SDRF). The reference platform hardware is two personal computers (PCs) with Intel Pentium™ processors, 10/100Mb network interface card (NIC), and full-duplex SoundBlaster sound card. Reference platform software includes Redhat Linux 7.2, Rational Rose Modeler, Sun Java JDK 1.4, GNU C++, and CORBA 2.3 [2].

Object Management Group (OMG) SCA Platform Independent Model (PIM). The PIM conforms to the OMG's Model Driven Architecture [3] (Fig. 2). A Request for Proposals (RFP) for the SCA PIM has been issued [4].

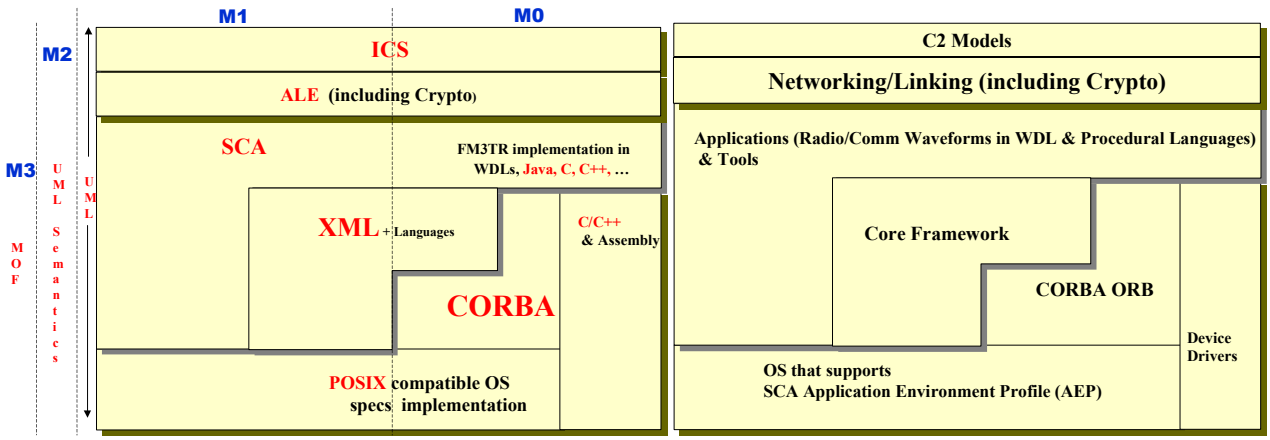

Fig. 1. The SCA is based on the Common Object Broker Architecture (CORBA). High-performance, minimal, real-time CORBA is needed to implement many software radios. In some instances, data parallelism is also a requirement.

Across the world, the competition to procure modern military radios is intense, and software-defined tactical radios are no exception. The SCA has been closely analyzed, and methods found to bring implementation costs to the absolute minimum, while still being specification compliant for JTRS Cluster One and other procurements. However, not all military radio systems can employ "minimum" software radio hardware and software configurations [5].

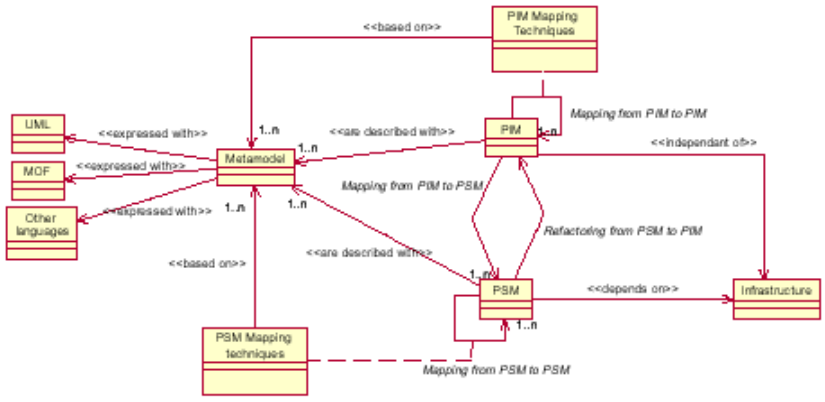

Fig. 2. MDA metamodel description for various enterprises. PIMs, PSMs and mapping techniques employ OMG core technologies, such as the Unified Modeling Language (UML). PSMs are defined for specific platforms, such as Java or CORBA. (Source: MDA Drafting Group, ormsc/2001-07-01, OMG Architecture Board ORMSC1, July 9, 2001)

Examples of applications requiring "scaled up" hardware and software include radios with specialized waveforms (e.g. ultra wideband modems, low probability of intercept/detection (LPI/LPD) modems), software radios jointly implemented with various space-time adaptive methods (co-site and co-channel interference cancellation, smart antennas), and software radios implementing spectrum monitoring or signal surveillance functions [5]. As the complexity of the waveforms and the platforms on which they are installed increase, the required processing power may increases from a few giga-operations per second (GOPS), to tens or hundreds of GOPS (Fig. 3).

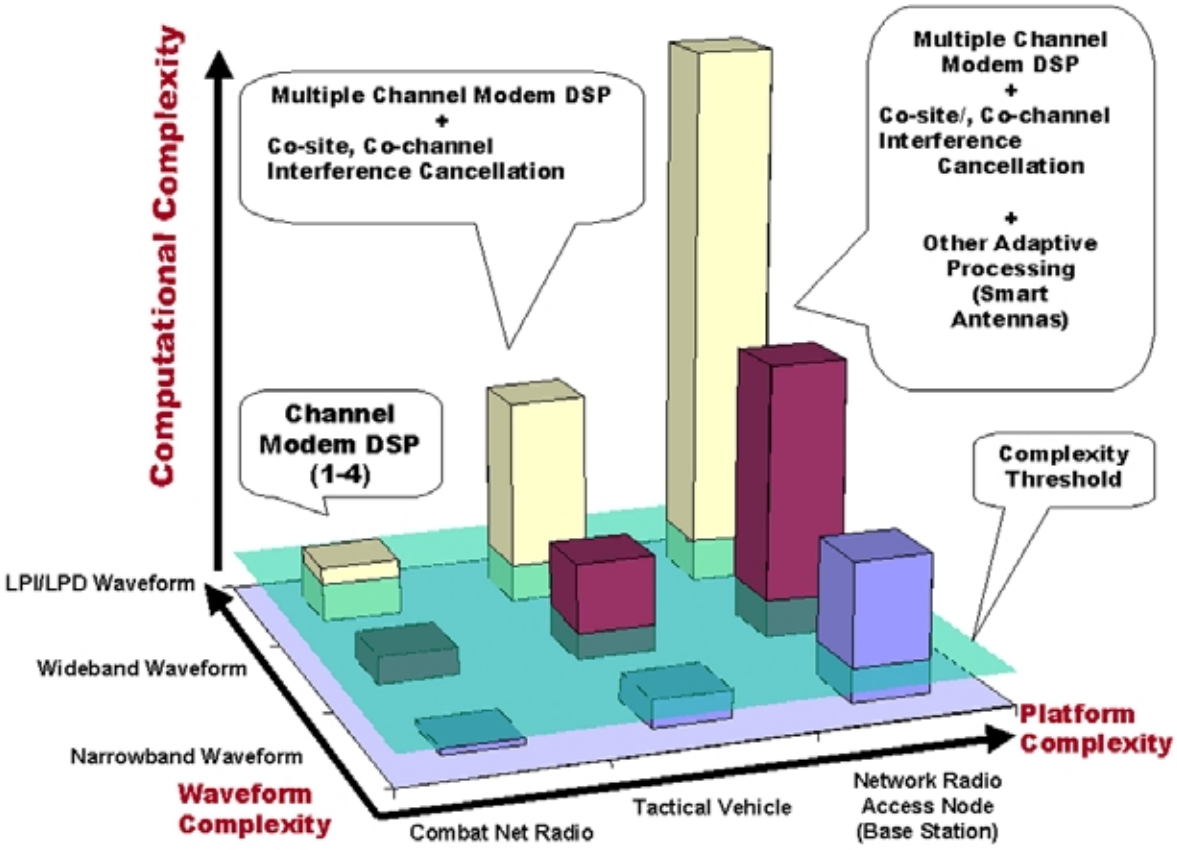

Fig. 3. Software radio signal processing computational complexity increases as a function of waveform and platform complexity. For several applications, especially those which combine multiple simultaneous transmissions and receptions on platforms of limited size, the computational needs of wideband modems, interference cancellation systems, adaptive antennas, and other needs increase the complexity threshold above the capability of the "basic" radio.

PROCESSING SCALABILITY REQUIREMENTS

On some military platforms, additional digital signal processing (DSP) may be required to implement high-performance modems, interference cancellation, adaptive equalization, or smart antennas. For instance, the need to simultaneously transmit and receive multiple signals – especially data signals – from small platforms (e.g. helicopters in flight) may lead to the requirement for co-site interference and electromagnetic interference cancellation [6]. Fig. 4 shows a functional diagram of an interference cancellation system for canceling co-site and electromagnetic interference on a helicopter with *i* transmitters, *j* receivers, and moving rotor blades. The *i x j* channel canceller requires a processing complexity comparable to an *i x j* channel space-time modem. For a software radio system processing a 5 MHz wide spread spectrum signal, the implementation complexity is may require approximately 100 GOPS to implement, some of which may require 32-bit or 64-bit floating point.

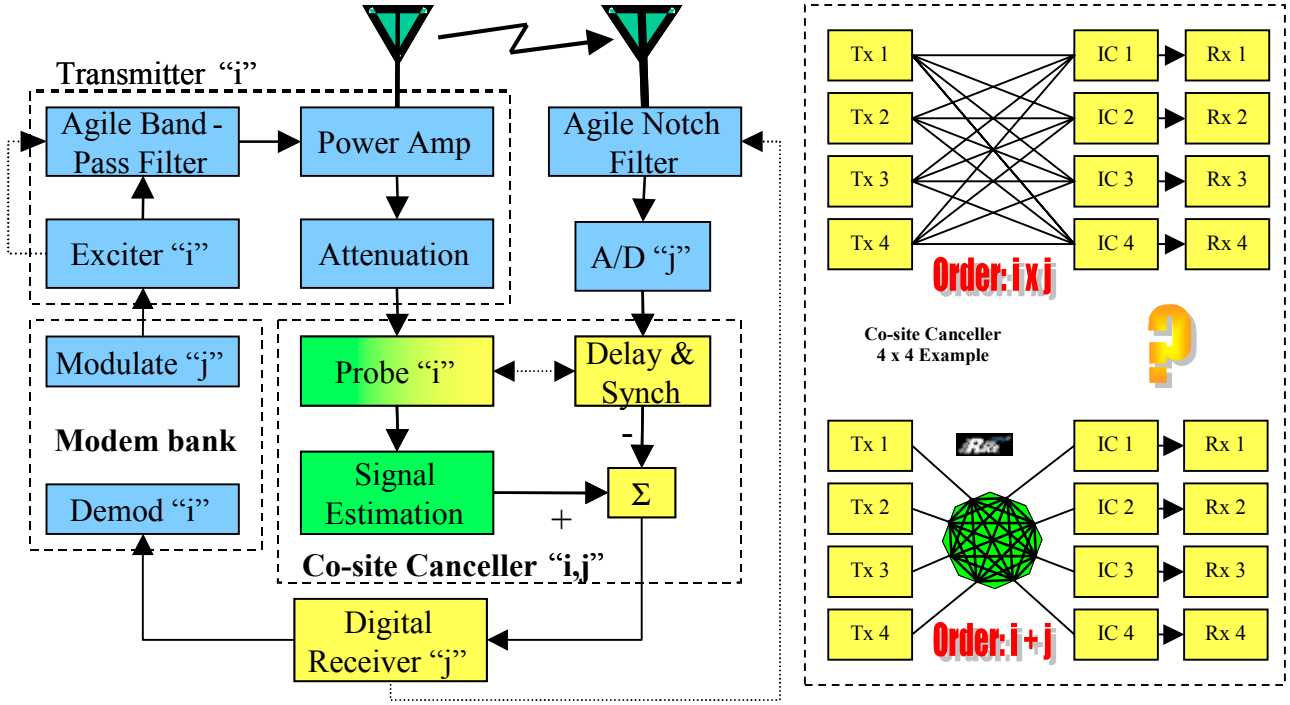

Fig. 4. Implementation of an integrated co-site and electromagnetic interference canceller may require up to 100 GOPS for defense platforms such as helicopters simultaneously transmitting and receiving up to four wideband signals.

Other applications, such as co-channel interference cancellation for spread-spectrum signals, or smart systems, also require adaptive processing systems that possess the following characteristics:

- Direct access to digital receivers signal flows at the chipping rate. By example, for CDMA signals, high-speed I/O must have access to the signals at a point between the rake finger receiver and maximum ratio combiner. [7]
- Processing requirements approaching 100 GOPS to implement multi-user detectors for wideband CDMA networks.
- Significant dataflow bandwidth. In the case of smart antennas or interference cancellers, the "I/O fanout" is typically of order [m x n]. In smart antenna arrays, m is the number of elements in an array, while n is the number of receiving channels to which the dataflow is directed. In interference cancellers, m is the number of interferers being cancelled, while n is the number of receivers being protected from interference. Further, the I/O bandwidth per data stream may be as much as 100-200 MB/s for wideband signals of 25-MHz bandwidth. A practical means of simplifying such quadratic dataflow problems is the use of switch fabrics with multi-port crossbars (Fig. 4).

Commonly, digital receiver and direct digital synthesizer implementations in software radios use re-configurable logic such as field programmable gate arrays (FPGAs) [8]. Thus, methods chosen to "scale up" signal and data processing in software radio systems implemented jointly with smart antennas and interference cancellation systems require a means to interface, in many cases, with combinations of FPGAs, DSP chipsets, and general-purpose processors (GPP) such as the Pentium or PowerPC.

SCALABLE PROCESSING AND DATAFLOW: A PRACTICAL METHOD

To achieve the dataflow scalability, use of conventional busses such as PCI are not viable. Conventional busses only support a certain limited number of endpoints. This forces the use of "bridges" to serve more than 4-8 endpoints, which is inadequate for most applications. By contrast, high-speed switch fabrics using crossbars, such as RACEway (ANSI-VITA 5-1994) or RapidIO, are ideal methods to implement multi-processing, heterogeneous "scale-ups" to an SCA-compliant software radio architecture (Fig. 5). Several high-performance software radio designs worldwide successfully employ combinations of PowerPCs and FPGAs interconnected with RACEway crossbars. Designs using RACEway and PowerPC/G4 compute nodes were successfully demonstrated in DARPA's Future Combat Systems-Communications (FCS-Comms) Phase 1 [9].

CONCLUSIONS:

Technology insertions, upgrading the I/O bandwidth and processing for needed processing upgrades, may be achieved by using the method shown in Fig. 5. In this fashion "baseline" radios, such as JTRS Cluster One, can be upgraded with high-speed switch fabrics designed for low latency, low jitter, and high bandwidth. Using open-architecture fabrics like RACEway, and POSIX compliant real-time operating systems (RTOS), SCA compliance can be maintained.

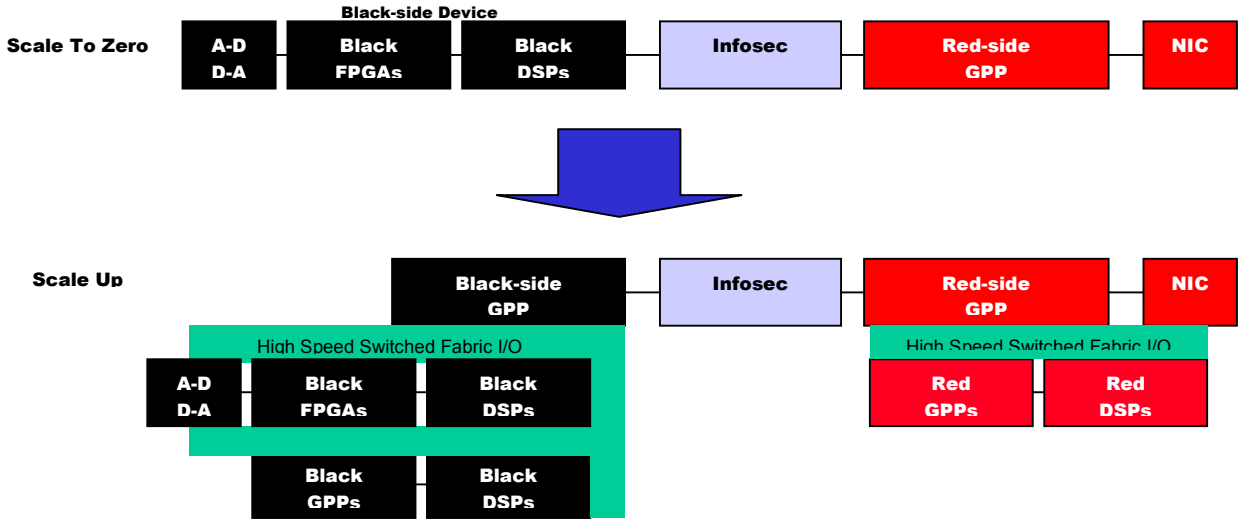

Fig. 5. Upgrading processing and dataflow bandwidths of SCA-compliant software radios with a Red-Black security architecture can employ high-speed switch fabrics like RACEway or RapidIO to replace conventional computer busses.

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