THE EFFECT OF GAUSSIAN NOISE ON A GENERIC COMPUTER BUS

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ABSTRACT

Computer buses are a building block of a computer. A bus consists of processors on each end of a line of one or many conductors. A processor will take information, process it, and transmit the results along a bus to another processor that checks the data for errors then further processes it. Noise on the line causes errors and those errors can cause failures in the system immediately or much later as the error correction methods are overwhelmed. This papers uses Shannon's theorem to predict a probability of error and impact of those errors are considered for a computer bus.

INTRODUCTION

Computers and computer networks make up a large fraction of the information infrastructure worldwide. Their susceptibility to a variety of electromagnetic stimuli is therefore of interest. Most analysis of electromagnetic susceptibility treats the problem in an analog radio fashion. That is, we compare the interference level of the to some threshold susceptibility field level and predict failure if the peak field of the interference is larger than the threshold. Digital equipment must be treated in a different way. In this paper, we first model the computer as a collection of data buses and consider the effect of the Gaussian noise interference as a means of increasing the bit error rate on those buses. Error detection and correction has the effect of slowing the operation of the buses more as the bit error rate increases. The response of the buses is of primary interest because they are the building blocks of a digital system and they have sufficient physical extent that they can act as antennas Maintenance of the data flow in the buses is critical to the continued operation of the computers.

APPLICATION OF SHANNON'S THEOREM TO ERROR PREDICTION

In the threshold analysis approach to immunity and related susceptibility testing, an electric field is applied to a test object and a result observed. Often, the center frequency of the signal is varied, but other parameters, like bandwidth and pulse repetition frequency are not varied. For later prediction, the analyst compares a peak electric field with the field level where some effect from interference to damage is observed. Better correlation with particular failure types might be found with, for example, the total energy in the pulse. Digital systems have the ability to recover from some errors, so that this model is not adequate for upset of digital electronics. Digital circuits also are likely to respond to a different norm of the waveform. In this paper, we will first examine some of the features of personal computers as they relate to their EMI and EMC response. We will then apply sufficient impressed fields (Gaussian noise) to cause a particular bit error rate. The bit error rate is calculated using Shannon's Theorem. Correction algorithms, as are sometimes used in the personal computer industry are then applied and the result noted.

The heart of a personal computer is its central processing unit (CPU). The CPU is connected to the rest of the system through a variety of buses. These buses are important to the EMI response of a computer for two reasons. The first is that they have a long extent (10 cm to meters) compared to that of the CPU alone. The second is that the signal characteristics of the buses are more consistent from one computer generation to the next than other parts of the

personal computer system. For example, the integrated system architecture (ISA) bus began with the Intel 80286 design and operates at a very slow 8MHz. Yet, rudimentary forms of the ISA bus can be found on the motherboards supporting 1 GHz Pentium III processors. Slow input devices, such as the mouse and keyboard, sometimes connect through the ISA bus or connecting electronics. The general characteristics of a bus are shown in Fig. 1. For example, the processor on the left takes information from another source and processes it. These data are sent along the lines to the next processor. During transmission, the data are subject to error.

The buses can be thought of as digital information circuits. Certain bit patterns are sent from a transmitter to a receiver to cause some action at the receiver. Receivers acknowledge receipt, check for errors and take corrective action. The two parameters that show problems with the buses are the bit error rate in the information circuit and the delay in message receipt caused by the error manipulation and repeat transmission caused by the error correction algorithms. Continued message repetition or other increases in overhead can cause system upset. Upset is an end state that we are attempting to predict using a model based on Shannon's Theorem for this type of system. The model is based on the theory presented by Kohlberg and Carter [Proceedings of the EMC Zurich Conference, Zurich, 2001]. Upset also can result from a bit change in the transmitter or receiver memory locations that control the data transmission parameters.

We use this model to predict particular failure levels in terms of signal to noise ratios for continuous Gaussian noise. The first example is for a computer mouse that has a very slow data rate and a simple error correction scheme. The second example is that of an ISA bus and is a more complex system. Most bus systems of this type have some type of error correction built in. A simple, but common, scheme is to examine the data sent and test it through checksums for errors. If an error is detected the receiving processor demands retransmission. The result of a series of errors (continuing noise) is that the operation of the bus is slowed. Sufficient slowing will cause upset of the bus and therefore the system. There are other error correction techniques, but they all show similar behavior at some level of signal to noise.

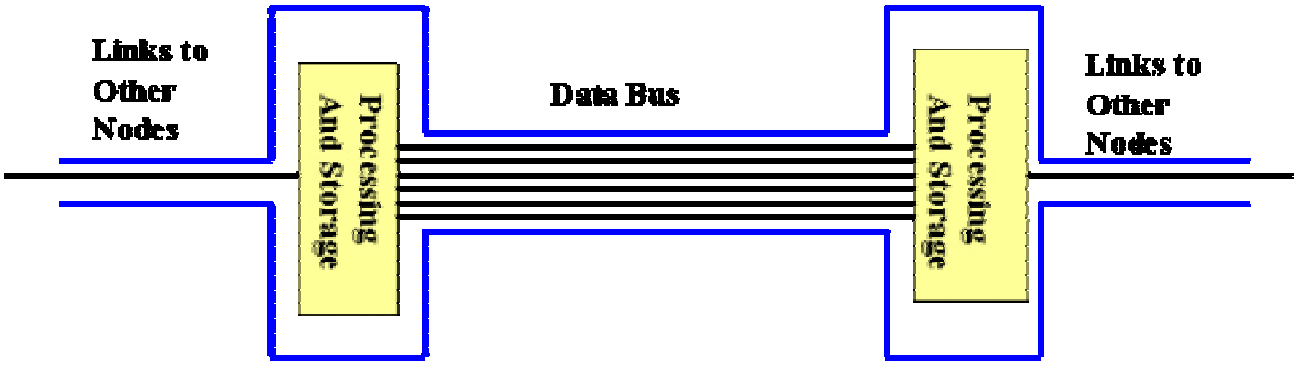

Figure 1: Generic Data Bus