

# Interconnects for a Multi-Layer Three-Dimensional Silicon Architecture

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## *I. Introduction*

Today's microwave and millimeter wave markets are driving three important metrics: low cost, high performance, and small size. This, in turn, dictates the replacement of traditional waveguide components, which are massive and costly but extremely low loss, with smaller semiconductor products. Solid state device technology has driven the development of planar Monolithic Microwave Integrated Circuits (MMICs) that dominate today's communications systems. This technology has allowed for the design of small radio frequency (RF) circuits that combine many functions on a single circuit while providing high performance and low cost. During the past two decades, the level of integration, available materials, batch-production yields, reliability, and raw performance of high-frequency and high-speed components have steadily increased. Consequently, many frequency and speed requirements previously met with large volume and/or weight components are now achievable with miniature, lightweight, and highly reliable devices.

Despite these advances, the development of MCM technology has clearly demonstrated the difficulty in realizing high power systems in monolithic form. The main reasons for this power limitation are low power MMIC devices, high-loss interconnects and passive components, low-efficiency planar antennas, and limited integration capability. The need to develop microwave monolithic circuits with high-power and low-cost leads to a number of requirements for optimum high-frequency performance: lightweight hardware, high-density interconnect technology, high reliability, and advanced packaging. The development of high-power microwave circuits with both small size and low cost poses serious challenges. The response to this challenge is to use novel concepts in circuit design, fabrication, and implementation to establish significant new benchmarks in power output.

## *II. A Multi-Layer Approach*

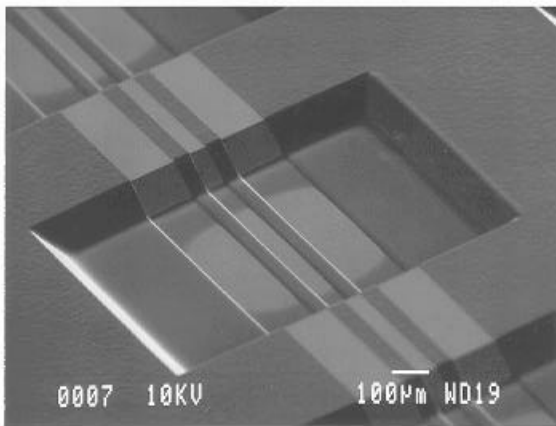
The next step beyond the current state-of-the art for the presently used multi-chip module (MCM) is the development of a technology which can provide monolithic integration of silicon (Si), or silicon germanium (SiGe) circuits, advanced micro-electromechanical (MEMS) devices, micromachined analog components (e.g. filter/multiplexers), and digital CMOS based

processing circuits into one wafer or multi-wafer stack. One way to meet the required metrics for both the microwave market and the semiconductor industry is a multi-layer approach. By replacing single chips, MCMs, and/or wafers with three-dimensional integration, substantial size and weight reductions may be achieved [1]. For example, a four chip stack requires less printed circuit board real estate as compared to four adjacent chips, improving substrate efficiency. With regard to power, a multi-wafer stack can provide more power per unit area than a single wafer in which sources and interconnects are on the same lateral plane. In addition, reducing the interconnect length through three-dimensional integration also improves performance by minimizing signal delay. The magnitude of these various benefits depends on the vertical interconnect and three-dimensional packaging.

MCM substrates may be cofired ceramic, printed wiring board, or a combination of thin film metals and dielectric materials over substrates such as silicon, diamond, and metal. Thus, at X-band and lower frequencies, there are many commercially available vertical interconnects for various multi-layer schemes on a number of substrates. Beyond K-band (20-30 GHz), and particularly at W-band (75-110GHz), this is not the case, and the examination of multi-layer approaches necessitates development of novel vertical interconnects. At microwave and millimeter-wave frequencies in particular, the added discontinuities of a vertical transition make low loss and wide bandwidth more challenging goals.

### *III. Silicon Micromachining*

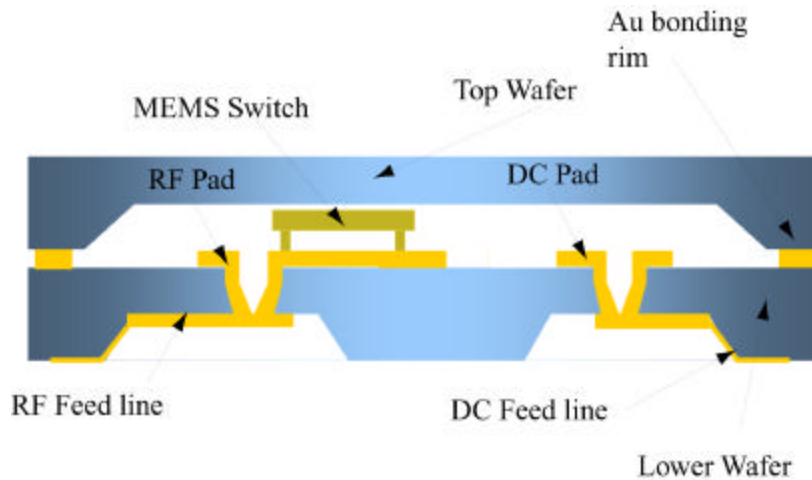
Silicon micromachining has been applied to microwave and millimeter wave circuits in many ways since its introduction in the late 1980's. Micromachining, or sculpting, of single crystal Si can be made by using either orientation-dependent (anisotropic) or orientation-independent (isotropic) etchants, as shown in Figure 1. Silicon supported transmission lines, and filters have shown improved performance and have extended the operating range of planar circuits to W-band frequencies and beyond [2,3,4,5]. In addition, silicon micromachined-based packaging, as shown in Figure 2, provides a high-isolation self-package, without the need for external carriers



*Figure 1: Silicon Micromachined Interconnects*

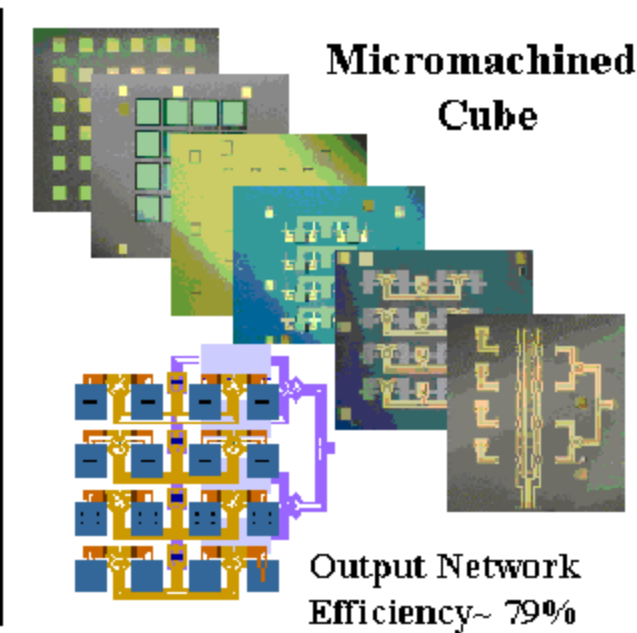
or external hermetic shielding. This method of circuit integration provides a comprehensive technique to integrate a very large degree of functionality on a single substrate with extremely high density and at a relatively low cost. The vertically layered structure of the micromachined circuit presents an excellent opportunity for three-dimensional integration, resulting in the potential for substantial reductions in size. Micromachined circuits are an ideal way to integrate MEMS (micro-electrical mechanical) devices and provide

components with performance and size advantages from 1 GHz to the terahertz regime. However, they demonstrate their greatest promise at K-band and above. Micromachining is truly an overarching master integration technology with the opportunity for an order of magnitude or more reduction in the size, weight, and cost of planar circuits, which can have a major impact on radar and communications applications in the military, commercial, and space arenas.



**Figure 2: Si-Micromachined Flip-Chip Package**

Micromachining techniques can be applied to any semiconductor substrate, but the use of Si



**Figure 3: W-Band Power Cube**

substrate layers as the foundation of the micromachined structure has major advantages in cost and the direct integration of SiGe and CMOS circuits. High resistivity Si also has mechanical, thermal, and electrical properties that compare well with the best ceramics, and as a result has been successfully demonstrated as the substrate of choice in three-dimensional integrated circuits [6]. Cost comparisons have been made for simple circuit applications and show one- and two-order of magnitude reductions in the cost of the same circuit packaged in ceramic. Circuit integration based on micromachined fabrication technology promises to be the key to achieving the very demanding cost, size, weight, and

simplicity goals required for the next advances in communications and radar systems for commercial, spaceborne, and military applications.

This paper focuses on Si wet bulk micromachining as applied to low loss planar transmission lines and multi-layer system integration techniques for ICs. After choosing an appropriate transmission line architecture for multi-layer applications, novel lateral and vertical interconnects will be presented. Packaging issues will be addressed before applying the interconnect technology to a W-band power cube transmit module application [7].

### *Acknowledgements*

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### *References*

1. S.F. Al-Sarawi, D. Abbott, and P.D. Franzon, "A Review of 3-D Packaging Technology," IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B, Vol. 21, No. 1, Feb 1998, pp. 2-14.
2. T.M. Weller, L.P. Katehi, and G.M. Rebeiz, "High Performance Microshield Line Components," IEEE Transactions on Microwave Theory and Techniques, Vol. 43, No. 3, Mar 1995, pp. 534-543.
3. R.F. Drayton, T.M. Weller, and L.P.B. Katehi, "Development of Miniaturized Circuits for High-Frequency Applications Using Micromachining Techniques," International Journal of Microcircuits and Electronic Packaging, Vol. 18, No. 3, Third Quarter 1995, pp. 217-223.
4. L.P.B. Katehi, "Si Micromachining in High-Frequency Applications", CRC Handbook on Si Micromachining, CRC Press, Boca Raton, FL, 1995.
5. R. M. Henderson and L.P.B. Katehi, "Silicon-Based Micromachined Packages for High-Frequency Applications," IEEE Transactions on Microwave Theory and Techniques, Vol. 47, No. 8, Aug 1999, pp. 1600-1607.
6. Katherine Herrick, Jong-Gwan Yook and Linda P.B. Katehi "Microtechnology in the Development of Dimensional Circuits", Invited Paper, IEEE Transactions on Microwave Theory and Techniques, Special Issue on Advanced Integration Schemes, Vol. 46, No. 11, November 1998, pp. 1832-1844.
7. K.J. Herrick, R.T. Kihm, and L.P.B. Katehi, "Interconnects for a Multi-Layer Three-Dimensional Silicon Architecture", 30th European Microwave Conference Proceedings, CNIT, La Defense, Paris, Oct 2000.