

RF TESTING AND MODELING OF WIRELESS COMMUNICATION DEVICES AND ICs

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ABSTRACT

Rapid development of high frequency devices and IC technologies for wireless communication products created many opportunities and challenges in RF testing, packaging and modeling. In this paper we review these challenges and show trends in the test and modeling technologies to meet the demand. Different approaches for studying large-signal performance of high frequency circuits, incorporating wave-propagation effects, will also be illustrated. Analysis techniques are based on finite-difference time-domain, interpolating wavelets, genetic algorithms, and circuit-based schemes. A fully distributed equivalent circuit model for power transistors will be presented. Advantages and limitations of the various approaches will be discussed.

INTRODUCTION

Over the past few years RF device and IC technologies have developed to such a level to allow manufacturing of low cost ICs with higher level of integration. In the past, the cost-driven nature of high volume opportunities favored a device or component level integration of the RF subassembly, which is the hybrid integration of discrete (packaged) semiconductors integrated with filters, crystals and other passive components on substrates. Now a paradigm shift towards monolithic integration is beginning to appear. Monolithic integration is being utilized to meet the demand for RFICs with reduced size and cost. Efforts to integrate the baseband circuits, antenna and RF selectivity with the RF front-end are being pursued by many companies. SiGe HBT technology combined with a CMOS fabrication process permits integration of a complete receiver function into a single chip. Similarly in the transmitter section, the predriver and driver amplifiers are being integrated into one circuit. Monolithically integrated GaAs single chip multistage power amplifiers, consisting of driver and output stages with on-chip tuning elements and inter-stage matching circuits are also being developed.

Rapid development of high frequency devices and IC technologies for wireless communication products created many opportunities and challenges in RF testing, packaging and modeling [1]. In this paper we review these challenges and show trends in the test and modeling technologies to meet the demand.

PROGRESS IN RF TESTING

Automatic RF testing has reached a high degree of precision over a broad spectrum of microwave device, component and system applications. Capability for on-wafer probing of both DC and RF parameters exists and is exploited to validate device models, monitor semiconductor process uniformity, and provide data needed for statistical process control and design centering, resulting in yield improvement. On-wafer power and noise figure measurements are routine, but require special attention to calibration techniques, probe design, and/or thermal control in cases of high power chips (>~5 W) or frequencies above ~40 GHz. Membrane probes have been developed for high-speed microwave multi-port measurements. In production, simple RFICs are typically screened at wafer probe using dc tests and then RF tested in their packages at final test. Complex RFICs, such as a transceiver, tend to be screened at wafer probe using RF functional tests, to save package scrap. Chips going into MCMs, hybrid assemblies, or sold as known-good die, are RF tested at the wafer level.

The speed of measurements for high-volume packaged RFICs is in the 1 to 2 second range for multi-function RFICs (i.e. LNA, downconverter) at a cost of \$0.10 or less per second. The high volume automation of RFIC testing, while it has improved greatly, is still a challenge. The package form factors, which make part handling difficult, and the

tighter placement accuracies required by RFICs makes RF part fixturing among the most difficult on the IC test floor. Recent improvements in device contactors (test sockets) will continue, driven by test needs at higher frequencies.

THROUGHPUT AND COST

Throughput and cost of test will continue to be the fundamental drivers. New test methods, elimination of marginally useful tests, and multi-site testing are just some of the approaches that will be used to lower cost. One trend is the need for more extensive digital and mixed-signal testing on RFICs, especially Si RFICs. Due to the high levels of integration permitted by Si, there will be an increasing amount of logic, low-frequency analog, and even memory testing in larger chips, which will be called SoCs with RF functions. Besides the challenge of the individual tests, there are the additional challenges of providing test access to various analog stages of the circuit, coordinating the various test subsystems, and completing all the tests in one to three seconds RF packaging will be driven by cost, size, and modularity. The test strategies used to achieve cost reductions to date include increasing the speed or reducing the cost of test equipment, eliminating redundant or unnecessary tests, testing earlier to eliminate scrap earlier and control processes better, testing devices in parallel to more efficiently use tester resources, testing unrelated parts of the chip simultaneously, and other strategies. Increasing the number of devices tested in parallel will likely continue to improve test throughputs and costs. Maintaining test fixture isolation sufficient for highly parallel test will be increasingly challenging as well. Accurate modeling and measurements of >100 dB isolation are required, for the cases of on-chip, chip-to-package, chip-to-fixture, and chip-to-chip through parallel wafer probes. Chip designers are developing their proprietary solutions, but the industry would progress faster if there were standard test structures, measurement tools and methodologies, modeling tools, and databases for high-isolation designs. As RF functions migrate onto system-on-a-chip (SoC), RF testing will have to be compatible with the logic, analog, and memory testing required by SoCs, including ATE, fixturing, and test time.

For high-volume parts, the production test costs for any given function is expected to fall at about 25 to 30% per year to remain competitive. To assure the required quality levels, virtually all RF components undergo at least a partial functional test at frequency at some point before shipping. As chips become more complex, production testing is done with powerful ATE systems that can test digital functions, IF or baseband analog functions, and RF functions, simultaneously when possible. Some simple RFICs are being tested two at a time today, and more parallelism is expected in the future. Power amplifiers for base stations are thoroughly tested and iteratively tuned before shipping. As linearity requirements become more stringent, new test methods will evolve with the new amplifier topologies. Evolving RF characterization and modeling measurement needs include further accuracy improvements at frequencies above 40 GHz, and better methods, test structures, design tools, and measurement capabilities for high-isolation measurements. Electrical isolation at high frequencies already limits integration levels of some SoC implementations.

RAPID PROTOTYPING

Rapid prototyping is essential in today's shortening product cycles. As such, simulation tools are key in being able to quickly evaluate options for a given design requirement. Several trends are emerging in regards to RF simulation tools. Merging of analog (RF) circuit design tools with system level and physical level designs tools are needed to shorten the product development cycle time. To accomplish this integration, the tools need to be seamlessly integrated with physical electromagnetic (EM) field and thermal simulators. For integration at the system level, mixed signal (digital/RF) simulation and integration of electrical design tools with mechanical design tools are required. Automatic circuit layout generation tools, layout verification systems (LVS) and design rule checking (DRC) tools are needed for RF and analog circuits to shorten the design cycle and to ensure first-pass success. A seamless framework and interface is still needed which extends from device to system (DSP level) and includes hardware elements such as modems and antennas. Mechanical, electromagnetic, thermal, analog, and digital effect integration will be necessary to simulate the system as a complete unit and allow tradeoffs between all design parameters. A transparent interface between the circuit design and layout is required to lower the cycle time and improve the accuracy of system level designs. Automated design rule checks capability in for RF and microwave circuit layout and subassembly fabrication is still in a rudimentary level compared to the sophisticated tools available in the digital world. Device and circuit libraries will necessarily extend to millimeter-wave frequencies.

MODELING, SIMULATION AND DESIGN

Several options are available to improving some aspects of simulation/design capability. Wavelet-based and multi-resolution techniques promise a ten-fold improvement in the simulation of electrical and thermal fields. Behavioral modeling at the system level allows complexity to be gradually introduced into a simulation model so as to optimize the trade-off between simulation detail and speed. Finally, genetic algorithms promise revolutionary improvements in the optimization of circuits and electrical structures when combined with the above mentioned simulation tools.

Different approaches for studying large-signal performance of high frequency circuits, incorporating wave-propagation effects, will be discussed. The circuits include high-frequency transistors. Analysis techniques are based on finite-difference time-domain, interpolating wavelets, genetic algorithms, and circuit-based schemes. An interpolating wavelet scheme is employed to solve the non-linear partial differential equations that characterize the behavior of semiconductor devices. Genetic algorithms are applied to solve Poisson's Equation, with the objective to relax the stability restrictions in hydrodynamic solutions. A fully distributed equivalent circuit model for power transistors will be presented. The distributed circuit model consists of several segments to accurately account for wave propagation effects along device width. The distributed model is analyzed in time domain, to retain the capability of evaluating large-signal behavior. Advantages and limitations of the various approaches will be discussed.

References

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