ON NEW TECHNOLOGIES AND SYSTEMS DEVELOPED FOR THE INTERNATIONAL *ATACAMA LARGE MILLIMETER ARRAY (ALMA)*

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ABSTRACT

The *ALMA* project is an array of 64x12-m antennas that will be remotely operated on a 5000-m high site in northern Chile in the (sub)mm wavelength domain. We briefly comment on some of the project technical decisions and the need for new developments. We then concentrate on the design of the *ALMA* broad bandwidth digitizers and digital filters. Finally, we give the main features of the Baseline and Second Generation cross-correlators required for *ALMA*.

THE *ALMA* ARRAY: MAIN SPECIFICATIONS AND TECHNICAL CHALLENGES

The Atacama Large Millimeter (and Sub-milimeter) Array (*ALMA*) project is an international collaboration with European, North American (and later Japanese) teams working jointly to construct and operate a unique instrument. This instrument will provide highly precise images of stellar and planetary systems in formation as well as precise images of nearby or primordial galaxies. The array comprises 64x12-m connected antennas which are moveable over an extent of about 14 km on a 5000-m high plateau in the Atacama desert of Chile. The extremely dry atmosphere of this remote site allows observations to the shortest possible sub-mm wavelengths (~ 300 μm). Each antenna will contain several superconducting, 4K-cooled receivers whose output data are digitized, transmitted through optical fibers, combined in a cross-correlator and further processed to provide astronomical images.

Some main characteristics of the *ALMA* project are given in Table 1. They are driven by the Science requirements listed in Chapter 2 of the *ALMA* Project Book [1].

Table 1. ALMA top level specifications

Number of Antennas	64 Cassegrain antennas, 12-m
Number of Interferometric Baselines	2016
Number of Antenna Stations	Transportable antennas, 250 Stations
Baseline extent	150 m to 14 km
Frequency Coverage	~ 30 - 950 GHz
Frequency Bands	10 bands, 4 first priority bands, 4K-cooling, photonic LOs
Intermediate Frequency (IF) Bandwidth	8 GHz x 2 polarizations (16 GHz IF per antenna)
Signal Transport	Digitization at antennas, optical fibre link
Bandwidth Selection	Digital filters at central laboratory
Correlator	Flexible configuration, 4 polarization products, thousands spectral channels, sub-arraying, etc.

Specifications in Table 1 have required intensive discussions. One may cite for example questions related to the photonic local oscillator (LO) generation in the receiver front-ends, selection of the IF, or digitization at the antenna or not. A simplified diagram (Fig. 1) shows the signal path to the cross-correlator which collects the data transported over optical fibers from all 64 antennas in the array to derive a maximum of 2016 interferometric complex visibilities.

The *ALMA* scientific objectives are extremely ambitious not only in scope but also in performances: extreme sensitivity (a few μJy in one hour in the continuum mode), very high spectral resolution (a few kHz), calibrated data at the one percent accuracy level, etc. Therefore, the technical specifications are difficult to meet and may require special design and development programs. In addition, many sub-systems require a large quantity production and a good repeatability of performances which can be achieved only with early industrial involvement in the project. Industrial partnership also helps to get round technological risks and improves the long-term reliability.

It is worth mentioning six technically challenging areas. *(1)* For the antennas a high quality series production must be achieved. In particular, the reflector surface accuracy goal is around 25 μm r.m.s., the pointing accuracy is 0.6 arc sec, and fast switching is required (1.5 degree in position in 1.5 sec of time). *(2)* The receiver IF bandwidth is broad (8 GHz per polarization) and the front-end receiver noise must reach a few quantum limits. Repeatability of

performances for all 64 receivers per frequency band is a difficult goal because of the great variety of involved elements (optical and mechanical components, electronics, cryogeny). *(3)* One must generate enough power at the photomixers to drive the receiver LOs without excessive phase noise level. (The basic scheme involves generation of a frequency ~ 100 GHz multiplied up at the antennas as desired.) *(4)* The 4 GHz-clock digitizers must deliver three bits and accept IF frequencies up to 4 GHz. Digitization at the antenna requires to transmit at least 96 Gbits/s and thus more bandwidth than in the analog transmission case (2x8 GHz) on two fibers. However, digital fiber optic link is preferrred for its higher efficiency and better gain stability. The system carries 12 optical signals each modulated at 10 Gbits/s. *(5)* Implementation of digital filters to narrow the IF is new in radio astronomy practice. *(6)* To process a large number of antennas and spectral channels the correlator requires innovative architecture and a new chip design.

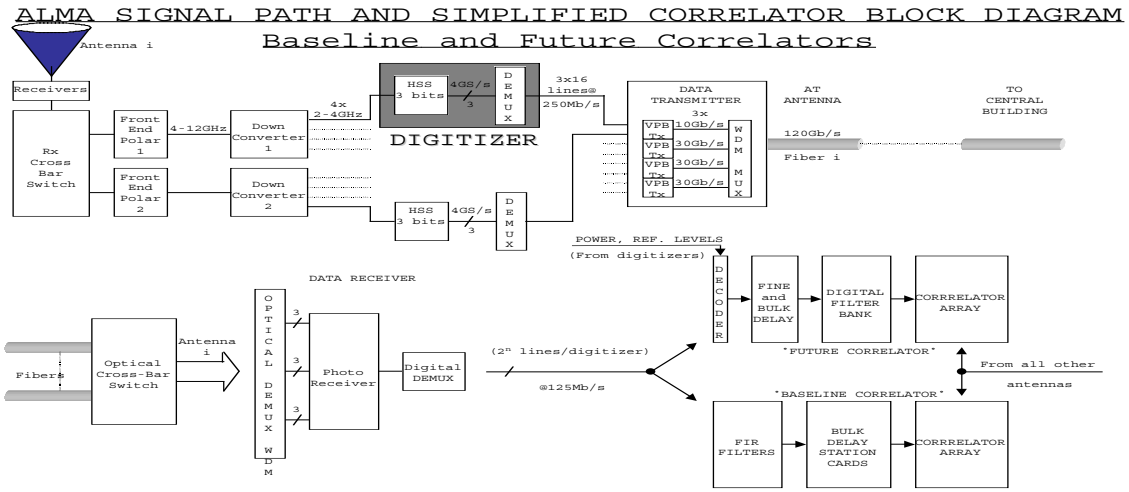

Fig. 1. Signal path from one of 64 antennas in the array to the correlator

In addition to the fabrication of several highly reliable sub-systems, several synchronization or stability problems must be resolved throughout the array. We mention two examples. The 64 antenna output signals must be processed simultaneously and thus a high stability of the fiber optic link is mandatory. This is achieved with an active loop to compensate for variations in the fiber. There is also an 'up-link' problem to resolve as we must carry the same reference frequency to all antennas to maintain a good instrumental phase coherence throughout the array. Supposing that we wish to achieve three degrees at 300 GHz between two atmospheric phase calibrations, then the stability of the fiber used for the frequency transport over 14 km must be around $4\ 10^{-10}$. This goal certainly requires frequent calibrations.

Management of a project as big as *ALMA* is also a challenge. All project areas are constrained by a fixed global envelope of about 570 M$ (fiscal year 2000) in the frame of the bi-lateral Europe-North America construction plan. In the antenna area for example the budgetary constraints mean that a low antenna production cost of about 30 k$/m^2 must be achieved; this is less than usual costs scaling well above the square of the diameter.

TECHNOLOGY DEVELOPMENTS FOR THE *ALMA* ARRAY

High Speed Analog-to-Digital Converters

Each of the 64 antennas contain 8 analog-to-digital converters (ADCs). The performance specifications are the following: input bandwidth = 2-4 GHz; sample clock = 4 GHz; bit resolution = 3 (8 levels); aperture time < 50 ps; aperture jitter ~ 2 ps; low power dissipation ~ 2 W. In our design we separate the sampling/quantizaion function (in the ADC) from the demultiplexing stage required behind the ADC to lower the input data rate to the digital filter and correlator. We thus minimize any potential coupling of the digitized outputs with the analog input signal and improve the SNR and dynamic range of the digital conversion stage. We have adopted a flash ADC architecture which is well suited to the conversion of broad bandwidths and to high frequency operation for a limited number of bits. Our designs are based on the SiGe BiCMOS 0.35 µm and 0.25 µm processes from STMicroelectronics [2]. They include CMOS transistors and SiGe bipolar transistors with 45 to 75 GHz transition frequencies. The power supply is limited to 2.5 V. We have designed several 2-and 3-bit ASICs to approach the *ALMA* specifications. The chips integrate an input adapter

amplifier, comparators followed by 2 latches, an encoding circuit and output buffers. The tests made on special PCBs with our first 2-bit designs show proper sampling up to 5 GHz clock and demonstrate that trade-off between low power consumption and 2 GHz-wide input bandwidth is possible [3]. Fig. 2 shows one of our 2-bit chip designs. The die area is 6.5 mm^2; this die was mounted in a VFQFPN36 package. A new 3-bit design with SiGe7 0.25 µm process has just been sent to the foundry for tests in the Fall. In addition, we have developed a special equipment to characterize our designs (auto-correlation and spectral analysis) and provide information to the ASIC design team (see [2]).

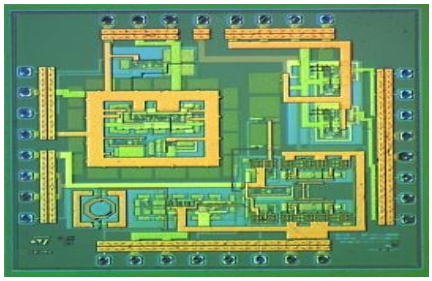

Fig. 2. Microphotography of the 2-bit ADC chip design of August 2001 (see [3])

The ADC delivers CML or LVDS differential logic levels at 4 GHz to a 1:16 demultiplexer which then delivers 48 LVDS lines at 250 Mbit/s to the *ALMA* optical fiber transmitter. One design uses commercial devices and a special synchronization circuit whereas another option is based on a specific chip development (triple demux for 3 bits).

Digital Filtering

Narrowing the processed bandwidth is required for spectral line analysis. This is made with analog filters, mixers and oscillators. For the *ALMA* project, digital filtering has been adopted to simplify the design, improve the reliability and costs and diminish a number of systematic errors. Finite Impulse Response (FIR) digital filters can be implemented with efficient tap weight multiplications and adder trees [4]. However, a second stage digitization (implying a loss of efficiency) is required because the correlators work with only 2- or 3-bit wide words. The main advantages of FIR filters are flexibility and stability. Flexibility is provided by the ability to change the weights in RAMs and to select any kind of filter shape. In fact, the in-band ripple, filter band slope and out-of-band rejection are inter-related and the performances depend on the number of taps implemented [e.g. 5]. FIR filters are stable with respect to environmental conditions (temperature) and their flat phase output response is especially well suited to interferometric applications.

The US team (NRAO) has tested prototype FIR filters which will be used with the *ALMA* Baseline Correlator. The passband performances (from 128 to 2048 taps in a single board with several Xilink chips for 1/2 to 1/32 band filter) and stop band attenuations (>30-40 dB) are documented in [6]. Most of the power in the filter card is dissipated in a few chips only and a technique is proposed to reduce the filter card power dissipation. The first prototype FIR filters made by the European team used 0.22 µm technology FPGA chips to implement several 32-tap FIR filters for 2-bit encoded input and output data. The FIRs can be cascaded to filter the input bandwidth by 1/2, 1/4 etc. with typical 0.4 dB in-band ripple and 30 dB out-of band rejection. In another prototype developed for 3-bit encoded input and output samples, a 64-tap FIR filter was implemented in a single ASIC [7]. The filter was developed with VHDL, built with CMOS technology and its functionnality (shift registers, multiplexers, adder tree) integrated in 25 mm^2. This demonstrator processes 20 MHz-wide signals with 8-bit encoded taps.

Implementation of >1024 taps in a single chip seems feasible. The biggest Xilink or Altera chips contain million gates with narrow processes and processes <0.10 µm will soon become available in high speed logic devices.

Baseline Correlator and the European Second Generation Correlator

In the XF correlation model the signal power is obtained by cross-correlating the independent antenna pairs of the array. The correlation products are then averaged and Fourier transformed to produce the astronomical images. Two correlators are shown in Fig. 1. The Baseline Correlator which is under construction by the NRAO team and the Future Correlator (or Second Generation Correlator) which is prepared in both Europe (see below) and Japan. The Baseline Correlator is described in Chapter 10 of [1] and meets the baseline science requirements. However, advances in semi-conductor technology (the number of components in an integrated circuit continues to double roughly every 18 to 24

months) and in correlator architecture (hybrid XF in Europe and at NRC-Canada, FX in Japan), and the need for always more spectral channels in many scientific programs make the planning for a future correlator necessary.

The major features of the Baseline Correlator may be summarized as follows. The design is for a XF-type lag correlator with a system clock of 125 MHz. The correlation format is for 2 bits, 4 levels, and there are 1024-lag and 1024-lead hardware cross-correlators per baseline. The NRAO correlator chip integrates 4096 lags each lag consisting of a 2-bit, 4-level, times 2-bit, 4-level multiplier. The power consumption in the 512 correlator boards is an issue because the heat is difficult to remove at a high elevation site. With low voltage technology the expectation is to dissipate less than about 1.5-2 W per chip thus improving the system reliability. NRAO aims at delivering a first correlator quadrant by mid-2005 to the *ALMA* site.

The European team works on the design of a 'digital hybrid XF' (Fig. 3) which is intermediate between the XF and FX architectures. The basic idea behind this design is to decrease the cross-correlation requirements by dividing the 2 GHz input baseband into a number of sub-bands. It is proposed to demultiplex the digitized 2 GHz-wide baseband signal with 32 digital filters. Sub-bands narrower than 62.5 MHz are possible by cascading the FIRs on a single board. Each sub-band is sent to a correlator board with 64 cascadable chips clocked at 125 MHz. The goal is to reach 8 kilolags per correlator chip for a 3-bit multiplication format. (The most modern processes and low voltage technology make it reasonable to envisage the integration of twice more lags than in the NRAO design.) The total number of spectral channels is an order of magnitude higher than in the NRAO design. As there are no technical show-stoppers in the European design, and following the development of digital filters and of a high frequency backplane demonstrator, the detailed designs of the FIR filter board and correlator chip have begun.

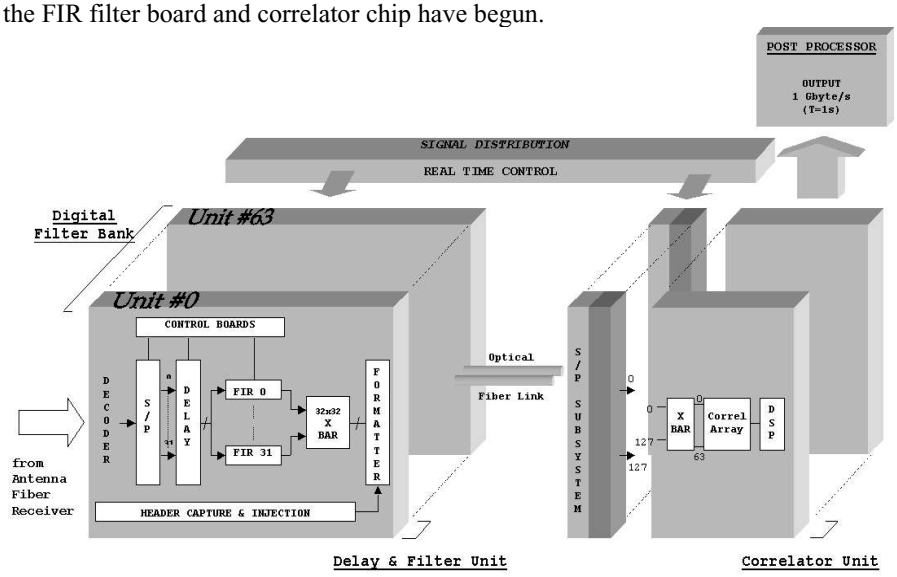

Fig. 3. *ALMA* Second Generation Correlator block diagram

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