TIME DOMAIN MODELING OF SILICON INTEGRATED SPIRAL INDUCTORS IN RF IC DESIGN

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ABSTRACT

A "full-wave" electromagnetic simulator for the analysis of solid-state spiral inductors in presence of lossy media, such as in CMOS technology, is presented. The EM numerical modeling has been used to determine the behaviour and discuss the basic loss mechanisms of planar inductors. Causes of loss and their relative importance have been discriminated and details of fabrication process have been correlated to actual device performance. Several integrated inductors have been fabricated and tested, allowing the validation of the 3D electromagnetic tool as a faster and cheaper alternative to experimental measurements. Finally, a clear characterization of RF-CAD compatible models has been possible.

INTRODUCTION

The widespread diffusion of wireless systems for personal telecommunications calls for a single-chip, standard-technology integration of low-cost, low-power, RF systems. Submicron MOS technology allows the implementation of active devices which may already comfortably operate into the RF frequency range; the integration of high-quality, solid-state passive components, however, is definitely more troublesome. In particular, inductors are key components for many subsystems in RF architectures, and mostly suffer from performance limitation coming from the adoption of microelectronic fabrication technology: the operating principle of such components is indeed basically three-dimensional, and is therefore inherently scarcely compatible with standard IC planar technologies. Integrated inductors are customarily obtained by patterning a spiral shape on a metal plane: in principle, building small-size, planar inductors is difficult because of the inherently non-planar behaviour of a coil (the magnetic flux being orthogonal to the current-flow plane) and of the lack of magnetic materials. Designing planar inductors thus results in large area consumption and in unwanted, yet unavoidable, interaction with adjacent layers: most notably, strong deviation from the ideal behaviour is usually due to the close proximity to highly-doped silicon substrates [1]. Experimental results show the poor performances calling for a deeper investigation. A sensible characterization of this behaviour, although being rather a difficult task, is hence of crucial importance.

In this work, we describe the application of physically-accurate simulation tools to the evaluation of integrated silicon spiral inductors: by means of three-dimensional, distributed electromagnetic field analysis, the inductor performance can be straightforwardly correlated to its geometrical peculiarities and to the fabrication process features. The performance of actual inductors has been correctly predicted and an automatic procedure has been developed for the extraction of equivalent-circuit components. This generic and process-independent approach generates lumped-element models that easily plug into the RF IC design flow. Their accuracy is established through comparison with measurements of fabricated test structures. By exploiting the capability of the "full-wave" simulator of making internal device fields and currents available, detrimental effects related to the specific technology adopted have also been evaluated and physically interpreted.

Even if, because of their inherent computational demand, "full-wave" analysis techniques can hardly be applied at the whole-chip level, they can be exploited, within a hierarchical design flow, to extract an accurate and physically-grounded characterization of compact, synthetic models of critical propagation regions. Thus a detailed understanding and evaluation of parasitics is made possible, allowing, in turn, the sensible characterization of compact CAD models to be used in the circuit design flow.

METHOD

The simulation scheme we adopt relies on the "full-wave" solution of Maxwell's equations, carried out by means of a "Finite-Difference Time-Domain" (FDTD) algorithm. This approach is based on the numerical, self-consistent solution of Maxwell's time-dependent curl equations and lumped element equations. To this purpose, the 3D space is divided in a finite number of elementary cells where electric and magnetic fields are mapped (forming the computational volume), while the time solution is obtained by an iterative scheme which evaluates the electric and

magnetic field components at alternate half-time steps. On the other hand, lumped element are incorporated into such a framework using the generalized Ampere's law. Features relevant to the application at hand include:

- non-uniform mesh spacing to avoid redundant node distribution [2];
- field absorbing boundary conditions have been imposed to account for field radiating out of the chip [3];
- the self-consistent solution of field equation with a network of external, lumped-element components (LE-FDTD, [4]) exploited here to account for a realistic signal source;
- de-embedding and parameter-extraction procedures, needed for the simulation-based characterization of SPICE models.

Our attention has been focused on silicon integrated spiral inductors suited for RF ICs. They have actually been fabricated using a standard CMOS process, i.e. Alcatel CMOS 0.35 μm and electrically tested, thus providing us with experimental validation of the modeling approach. The basic inductor, depicted in Fig.1, is obtained by a square spiral pattern, featuring two turns on the upper layer and a return path on the underlying layer. The metal wires are insulated from the silicon layers by a SiO_2 layer. Below the oxide, the considered fabrication process features an epilayer and a rather conductive thick silicon substrate. The semiconductor layers are modelled as linear media and have been characterized by a doping-dependent electrical conductivity. The SiO_2 layer is assumed to behave as an ideal dielectric material. Metal and polysilicon layers are assumed of finite conductivity to account for ohmic losses. The analysis proceeds as follows: first, a wide-band Gaussian pulse is applied to the inductor using the lumped voltage generator (internal resistance equal to 50 Ω)[4]. The other port of the inductor is maintained at ground potential during the analysis. Then, full-wave propagation of the pulse, which inherently accounts for parasitic paths of any kind, is simulated by the FDTD algorithm, providing the time-domain inductor response. As a post-process option, the impedance spectral components are extracted by applying a DFT transform. From these components, the actual equivalent inductance, resistance and quality factor are eventually computed. Furthermore, the extraction of frequency-domain field and current surfaces on arbitrary cross-sections is available in order to study the eddy currents paths and the penetration of electric and magnetic fields into the lossy substrate.

RESULTS

Measurements have been carried out at the wafer level by means of an HP 8720 network analyser and a probe station with GSG-pattern probe tips featuring a 150 μm pitch. The device has been embedded in a coplanar test structure, as shown in Fig. 2a, with pad dimensions of 100×100 μm. The SOLT (Short-Open-Load-Through) calibration procedure has been performed by means of a standard calibration substrate. Finally, a pad de-embedding procedure has been carried out, using an integrated open structure,shown in Fig. 2b. The overall agreement between measurements and simulation results is good, in terms of peak quality factor (Q) and self-resonance frequency (see Fig. 3). The critical impact of parasitic phenomena reflects on rather poor values of Q (if compared with technologies more explicitly oriented to high-frequency applications, such as GaAs).

The peculiar shape of the resulting curves can be interpreted by looking at asymptotic limiting factors. At low frequency, the dominant factor consists of the non negligible series resistance of the coil (due to the finite conductivity of aluminium and to the small cross-section). As the frequency grows, substrate losses tend to gain importance, prevailing close to the self-resonance region, where the inductor behavior turns into a capacitive one and have different origins. At high frequencies, the current, in fact, is no longer confined into the metal pattern: displacement currents become more and more significant, as shown in Fig. 4 ,being particularly evident in the inter-turn gap, pointing out the progressive coupling among adjacent legs. The coil, at increasing frequencies, tends to behave as a conductive plate, capacitively coupled with the substrate.

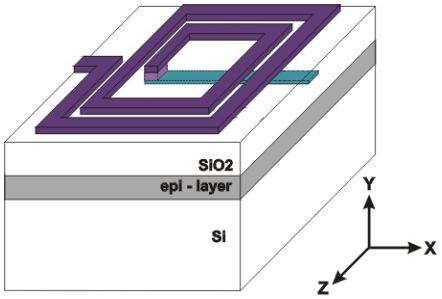

Fig. 1. Sketch of the standard simulated spiral inductor

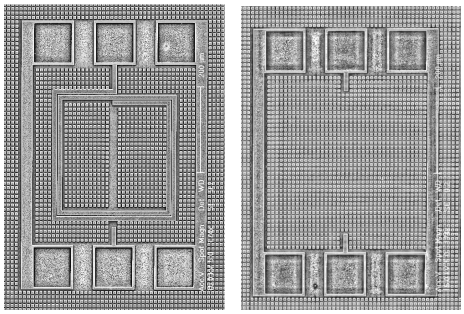

Fig. 2. SEM micrograph of the simulated inductor (a) and of the test structure for PAD de-embedding (b)

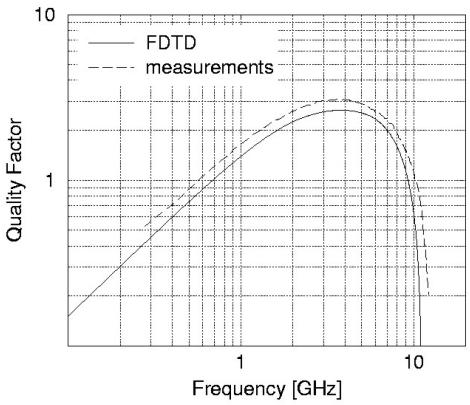

Fig. 3. Simulated and measured Q-factor for the CMOS spiral inductor

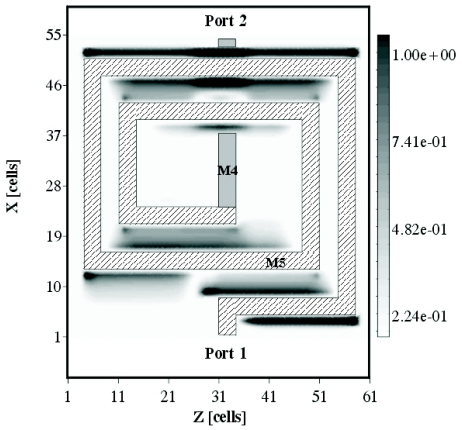

Fig. 4. Cross-sectional view of the normalized modulus of x-component conduction current @10 GHz

A further loss mechanism is due to the penetration of the magnetic flux concatenated with the spiral into the silicon which induces some concatenated "eddy" current to flow into the substrate itself, thus further dissipating energy as shown in Fig.5.

EQUIVALENT CIRCUIT

The design flow of complex Si-RF integrated circuits heavily relies on CAD tools: among them, circuit simulation plays a fundamental role in analysing the behaviour of analog (or mixed-signal) circuits. It is of the outmost importance, therefore, to provide circuit simulators (e.g., SPICE or microwave oriented ADS) with accurate, yet computationally affordable, models of the integrated devices. These models, as well as the FDTD approach, should account for actual technology parameters. A CMOS process in fact is optimised for digital applications, which hardly suffer from technology corners [5]. By contrast, due to electromagnetic phenomena taking place in the three-dimensional structure, analog applications are extremely sensitive to the fabrication process, thus models must assure that the designed inductor will perform as predicted. In this contest, a significant aid may come from the FDTD approach, which can easily correlate the inductor behaviour with process parameters.

The maximum and the minimum resistivity and thickness for the metal layers and the substrate are simulated and compared to the typical values. As expected the results shown in Fig. 6, demonstrate a great influence of such parameters on the inductor performance.

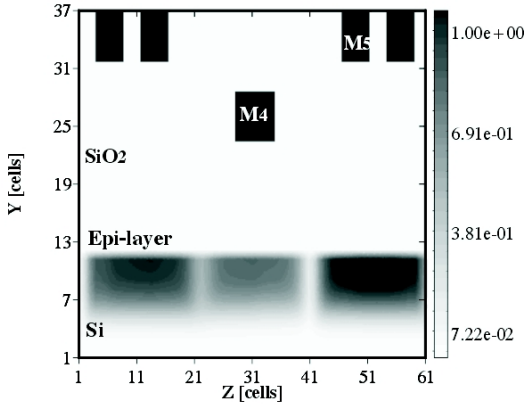

Fig. 5. Normalized modulus of x-component dispacement current within the oxide @10 GHz in a planar section

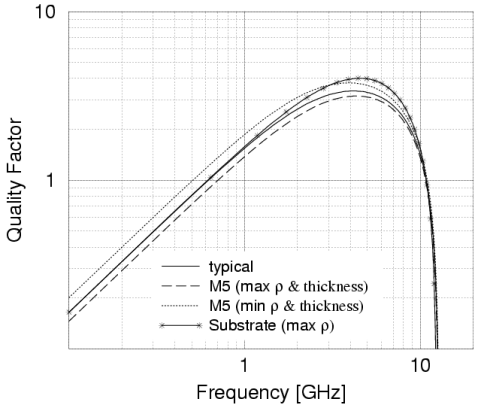

Fig. 6. Simulated sensitivity of a standard inductor to metal layers and substrate process parameters

On such a basis, starting from simulations, we have extracted the model parameters, being sure to account for process latitude. With reference to silicon-integrated inductors, several authors [6] have investigated such an issue, proposing lumped-element equivalent circuit topologies: by means of the distributed simulation approach introduced above, characterization of the model parameters can be carried out in a virtual environment, avoiding the need of an *a posteriori* experimental parameter extraction. Starting from simulated data, a two-step optimisation procedure has been carried out on the parameter values: first, a least-square fitting procedure has been performed by means of a dedicated program; then, parameters are more finely adjusted by using a commercial circuit optimiser. The good agreement between the ADS (Advanced Design System) and the FDTD simulation shown in Fig.7, demonstrates the accuracy of the proposed approach, which can, hence, be safely used to extract the equivalent circuit parameter values for the considered inductor accounting for process latitude.

CONCLUSIONS

In summary, by resorting to 3D numerical solution of Maxwell equations, we were able to predict quite accurately the behaviour of actual planar integrated inductors and to evaluate the impact of some technological and design options. Among the advantages of such an approach, it is worth remarking its contribution to the physical and intuitive interpretation of the actual device behaviour. This allowed, within a context which inherently suffers from an intricate set of interacting parasitic phenomena, for the comprehensive evaluation and discrimination of basic degradation effects. The good agreement obtained between measurements and simulations demonstrates that the developed virtual environment, capable of accounting for both technology and design layout parameters, is a useful, cheaper than fabrication, aid for the extraction of compact device models, suitable for commercial CAD packages.

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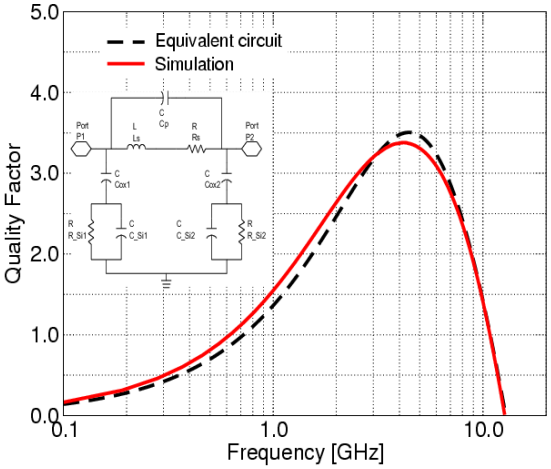

Fig. 7. Comparison between simulated quality factor and ADS simulation of the circuit shown in the inset