FDTD Modeling of Void Defects in VLSI Interconnections

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I. Introduction

One of the limiting factors to the reduction of interconnection wiring dimensions in Very Large Scale Integrated circuits (VLSI) is voiding damage due to both electro- and stress-migration. Indeed, under the influence of high current density or mechanical stress the ions of the metal lattice will drift inducing void-like defects in the metal line. Purpose of this work is to numerically estimate the impact of metal-voiding on the frequency-dependent transmission line parameters of an interconnection. In particular, a three-dimensional electromagnetic simulator, based on the Finite Difference Time Domain (FDTD) method, has been exploited and the transmission line parameters of a particular high-frequency CMOS interconnection have been derived in a wide (DC to 100 GHz) frequency range.

II. Method and Results

The cross-section of a typical, high-frequency, CMOS interconnection is quite complicate because of the presence of the semiconductor substrate and passivation layers. A simplified model of such structure can be obtained considering a signal line running between two return (ground) lines connected directly to the conductive Si substrate by a continuous grid of stacked vias. Geometrically, these lateral ground lines have been modelled by enclosing the cross-section within a metallic box as in Fig. 1(a).

The resulting transmission line can be described in terms of four, frequency-dependent, electrical parameters, namely: the inductance, the capacitance, the resistance and the conductance per unit length. These parameters can be evaluated by accurately computing the characteristic impedance and the propagation constant of the line.

To this purpose our three-dimensional FDTD simulator [1] has been used. This approach allows us to deal with uniform structures (unperturbed in the direction of propagation) as well as with damaged interconnections. The latter have been modelled assuming void-like defects along the signal line, thus simulating the presence of stress-induced voids. In particular, rectangular shaped defects have been considered, alternated to the left and to the right side of the line.

The wide-band evaluation of the line parameters is quite a challenging task: for example the specific resistance is particularly sensitive to numerical errors in the phase of the characteristic impedance. To improve the accuracy of the results, a Short-Open Calibration(SOC) technique has been used along with the FDTD simulator. This technique, originally developed in [2] for the Method of Moments (MoM), has been adapted to our FDTD algorithm.

To validate the proposed approach, the CMOS interconnection experimented in [3] has been considered. This structure (access line) is fabricated in the second level of metal and features a thickness of $0.7\,\mu$m and a width of $1.0\,\mu$m. The conductivity of the silicon substrate is $10^4\,$S/m.

The interconnection has first been assumed unperturbed (defect free) and has been simulated with the FDTD method. Then the SOC procedure has been applied and both the characteristic impedance and the propagation constant have been computed. A comparison between these results and the measurements reported in [3] shows a good agreement.

Having checked its accuracy, the proposed approach has been used to investigate the wide-band electrical properties of voiding damage in CMOS interconnects. To this purpose 11 defects of size $0.75\,\mu\text{m} \times 0.75\,\mu$m have been distributed along the line. The distance between two defects is $5\,\mu$m. The specific resistance and conductance evaluated in this case are compared against the parameters

for the unperturbed line, see Fig. 1(b). From the analysis of these results emerges that only the series resistance is sensitive to the defects. The other line parameters and, in particular, the conductance are only slightly affected. The latter, indeed, is associated with the substrate conductivity which is very high. A second set of simulations have thus been carried-out with the substrate conductivity equal to $10^2\,\mathrm{S/m}$ (100 times less than in the previous case). Although the line conductance increases of about 10 times it remains slightly affected by the voiding damages.

Future work will deal with a comparison between FDTD simulations and experimental results from a recently published high frequency technique for detecting voiding damage [4].

References

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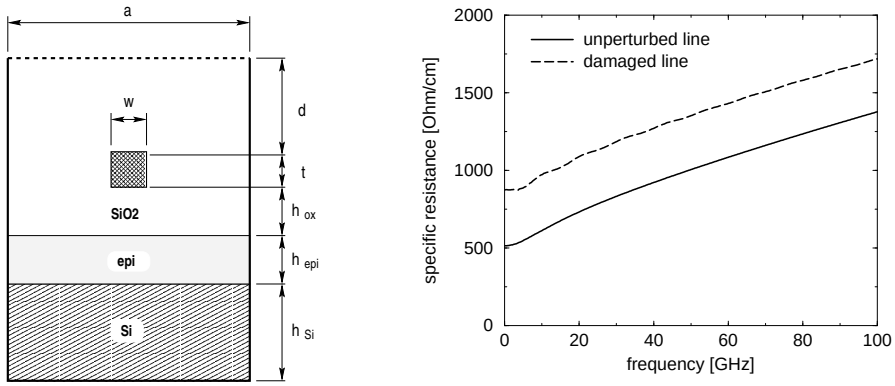

(a) structure (b) results

Fig. 1. Reference CMOS structure (a) and comparison between unperturbed and damaged interconnections for $\sigma_{Si} = 10^4\,\mathrm{S/m}$ (b). The other cross-section parameters are: $h_{Si} = 508\,\mu\mathrm{m}$; $\epsilon_{Si} = 11.7$; $h_{epi} = 4.2\,\mu\mathrm{m}$; $\epsilon_{epi} = 11.7$; $\sigma_{epi} = 10\,\mathrm{S/m}$; $h_{ox} = 2.9\,\mu\mathrm{m}$; $\epsilon_{ox} = 3.9$; $d = 8.6\,\mu\mathrm{m}$; $t = 0.7\,\mu\mathrm{m}$; $w = 1\,\mu\mathrm{m}$; $a = 130\,\mu\mathrm{m}$; $\sigma_{Al} = 27.8 \times 10^6\,\mathrm{S/m}$.