Applications of Calibration Comparison in On-wafer Measurement*

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ABSTRACT

In this paper we discuss several applications of calibration comparison in on-wafer measurement. This technique can be understood as an abstraction of the well-known two-tier deembedding scheme used in test-fixture characterization. The applications presented here include the assessment of accuracy of a given on-wafer calibration with respect to a benchmark calibration, the compensation for substrate permittivity in probe-tip calibration, the determination of characteristic impedance in planar transmission line structures, and multiport calibration.

INTRODUCTION

The calibration comparison method for on-wafer calibrations [1] is based on two-tier calibration [2] and determines two matrices (the "error boxes") relating the two on-wafer calibrations. Typically, these matrices represent the relationship between a first- and a second-tier calibration. Once these matrices have been determined, several important quantities can be derived that quantify the systematic differences between the two calibrations. Most important are changes in the reference plane position and reference impedance, but also worst-case measurement deviations of any calibration relative to a benchmark calibration can be calculated [1]. For example, [1] shows how to determine an upper bound for $|S_{ij} - S'_{ij}|$, where S_{ij} and S'_{ij} are the S-parameters of any passive device measured by the benchmark calibration and the calibration under investigation, respectively. This allows the differences between calibrations using different types of standards to be quantified.

TEST-SET DRIFT AND INFLUENCE OF SUBSTRATE PERMITTIVITY

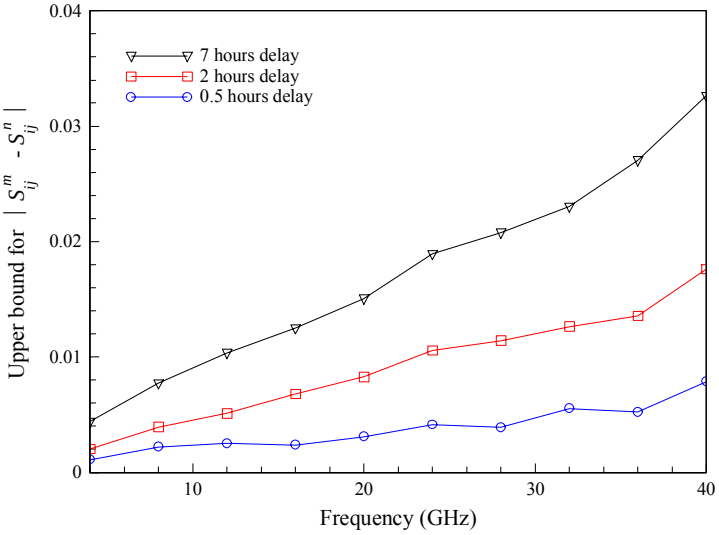

Fig. 1. Worst-case differences between calibrations performed with identical artifacts as a function of elapsed time. (From [3].)

If we calculate the worst-case differences between calibrations performed with identical artifacts as a function of the elapsed time between calibrations, we can quantitatively assess the influence of connector repeatability and drift in the vector network analyzer (VNA) setup used to perform scattering-parameter measurements [3]. Fig. 1 summarizes results obtained from comparing calibrations performed at different times when using the same artifacts. Each calibration was performed as a multiline TRL calibration [4] in CPW lines of different lengths built on a GaAs wafer.

In [5] the calibration comparison method of [1] was used to quantify the differences between multiline TRL probe-tip calibrations

performed with artifacts built in virtually identical geometry but on different substrates. Fig. 2 shows the upper bounds on $|S_{ij} - S'_{ij}|$ for ij ∈ {11,12,21,22} for calibrations performed on lanthanum aluminate, silica, and sapphire substrates when compared against a benchmark calibration performed on a GaAs wafer. Plotted in dotted lines is the bound for two nominally identical GaAs calibrations performed at the beginning and end of the experiments, which is a measure for instrument drift and contact errors (cf. Fig. 1). [5] also shows that the systematic differences of Fig. 2 due to different substrate permittivity can be compensated for by modelling the end effects at the CPW lines as a small shunt capacitance at the probe tip. Fig. 3 shows that, after compensating for the differences in the shunt capacitances, accuracies similar to the GaAs benchmark calibration can be achieved on all the different substrates investigated.

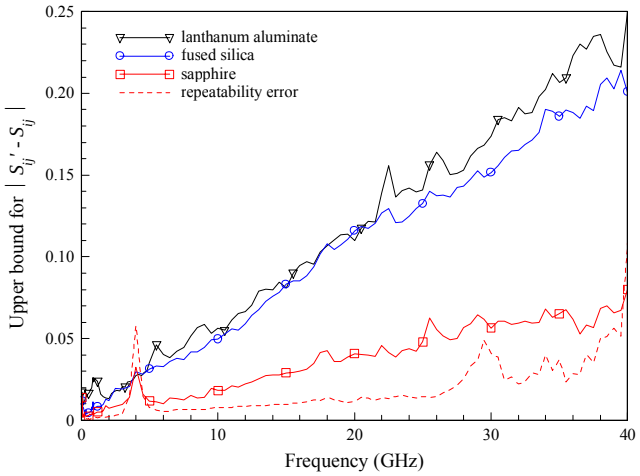

Fig.2. The bounds for differences between measurements of passive devices using calibration on different substrates. (From [5]).

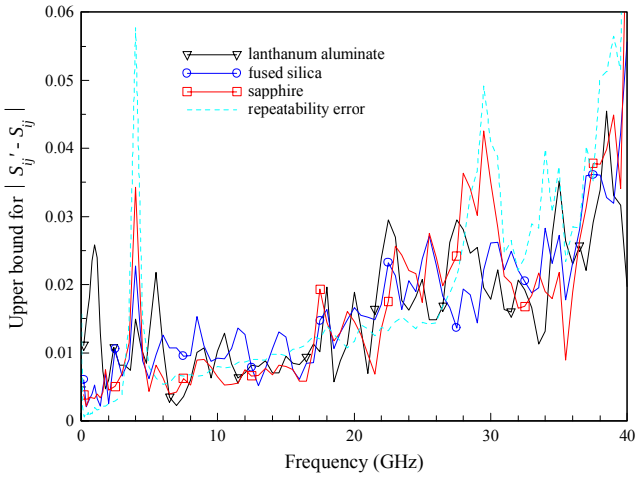

Fig. 3. The bounds of Fig. 2 after applying the substrate permittivity compensation described in [5].

CHARACTERISTIC IMPEDANCE DETERMINATION

Another important application of the calibration comparison method is the determination of the characteristic impedance Z_0 of planar transmission lines printed on lossy substrates [6]. Z_0 can be found even when contact-pad capacitance and conductance are large. The method begins with the performance of a multiline TRL probe-tip calibration [4] in a set of easily characterized reference lines. The reference impedance of this calibration is set to 50 Ω, and its reference plane is moved back to a position close to the probe tips. A second-tier multiline TRL calibration in the transmission lines of interest determines the error boxes relating it to the 50 Ω probe-tip calibration. Reference [6] suggests a different treatment of the error boxes determined by [1], which is insensitive to contact pad parasitics and is well suited for determining the characteristic impedance on lossy substrates.

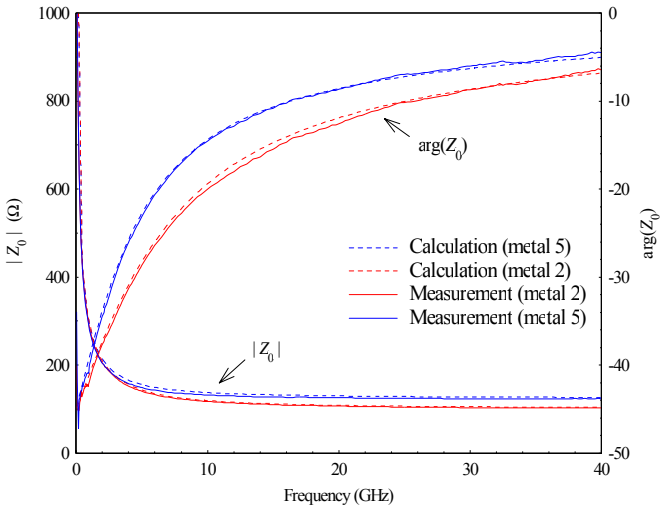

Fig. 4. Characteristic impedance of 1 µm wide lines built in different metal levels of a 0.25 µm CMOS technology. (From [7].)

Fig. 4 shows the measured characteristic impedance of 1 µm wide lines built in the second and fifth metal level of a six-metal-level 0.25 µm CMOS technology [7]. The measurement is compared against the quasi-analytic calculations of [8] and shows excellent agreement over the whole frequency range of 40 GHz.

MULTIPORT CALIBRATION

Finally, we demonstrate how two-tier deembedding [2] can be used to implement a multiport calibration scheme with a minimum number of inline calibrations. Here, we use the error boxes determined by calibration comparison to map measurements corrected with respect to one calibration onto measurements calibrated with another calibration. Most important in the context of multiport calibrations is the change in reference plane location, but changes in the reference impedance can also be accounted for. We use the 4-port setup introduced in [9] to illustrate the procedure (see Fig. 4). The switch configuration shown in Fig. 4 connects port one of the analyzer to the south probe and port two to the north probe. The east and west probes are each terminated in 50 Ω.

In the multiport calibration and measurement procedure of [9], two-port calibration standards are first connected between the east and west probes. Subsequently, this calibration is used to correct all the raw measurement data to reference planes at the east and west probe tip. Then, the two-port calibration standards are connected between the north and south ports. These second-tier calibrations performed in south-north and north-south direction are related to the initial west-east calibration by a set of four "error boxes". These error boxes map measurements corrected to the west and east on-wafer reference planes to measurements at the north and south reference planes. Reference [9] also describes how the imperfect termination impedances can be accounted for and how the corrected two-port measurements can be used to derive a four-by-four S-parameter matrix with a reference impedance of 50 Ω at all ports.

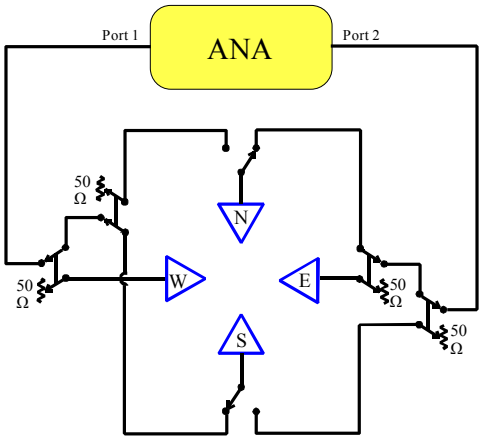

Fig. 4. Four-port measurement system schematic of [8].

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