

SUSCEPTIBILITY OF DIFFERENT SEMICONDUCTOR TECHNOLOGIES TO EMP AND UWB

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ABSTRACT

In this paper the influence of the technology on the breakdown and destruction effects of semiconductors by impact of EMP (Electromagnetic Pulse) and UWB (Ultra Wide Band) pulses is determined. Different logic devices like NANDs and Inverter were exposed to high amplitude transient pulses and new definitions were introduced to describe effects and thresholds.

I. INTRODUCTION

The goal of this investigation is to measure the susceptibility of electronic devices to a transient electromagnetic field threat. Modern electronics are of vital importance for the function of traffic systems, security systems and modern communication. A malfunction in one of these areas could cause casualties and economic disasters. Nowadays HPM and UWB equipment can be bought by everyone. Taken the aspect of electromagnetic terrorism into account an UWB system could be a very dangerous weapon, because it can be built in a very small volume due to the low energy content of the pulse. Therefore the susceptibility of electronics to pulsed electromagnetic fields like EMP and UWB pulses is of great interest. The intention of this work is to analyze the influence of the semiconductor technology on the breakdown and destruction effects. On that account ten different technologies (six TTL- and four CMOS-Technologies) have been tested.

II. GENERAL MEASUREMENT SETUP

The applied pulseshape is generally double exponential as shown in Fig. 1a. Five different pulse generating devices are available. Fig. 1b shows the rise time (t_r) and the full width half max value (t_{fwhm}) of the different pulses.

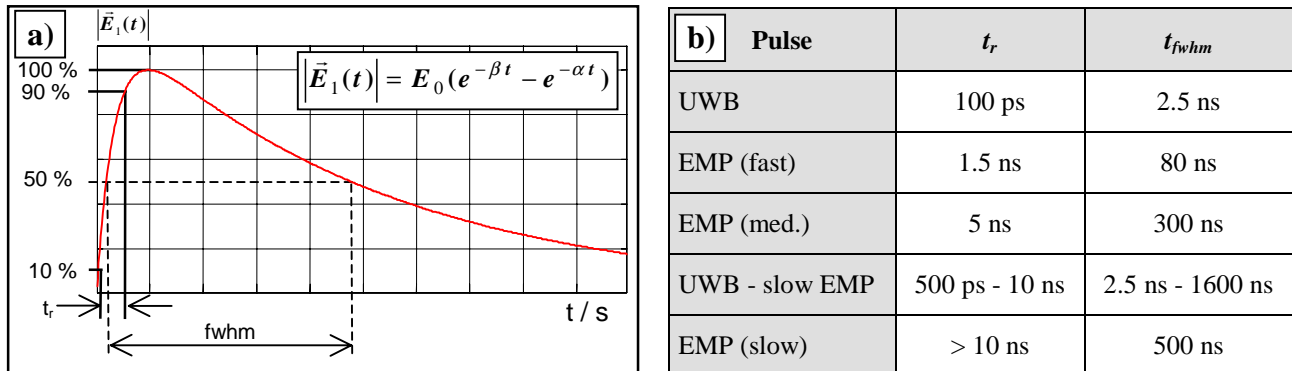


Fig. 1. Pulseshape (a) and Pulseparameters (b)

The measurements were carried out with two different waveguides shown in Fig. 2. Waveguide 1 (Fig. 2a) is an open area test simulator with a maximum height of about 23 m described in [1]. Waveguide 2 (Fig. 2a, described in [2]) is an open waveguide inside a shielded room enclosed by absorber walls. The absorbers at the end of the waveguide were placed on interchangeable wooden walls. The position of the septum can be adjusted via nylonthreads. The

measurements of the electromagnetic properties were done by a Time Domain Reflectometer (TDR) and electric and magnetic groundplane and free field probes as described in [3].

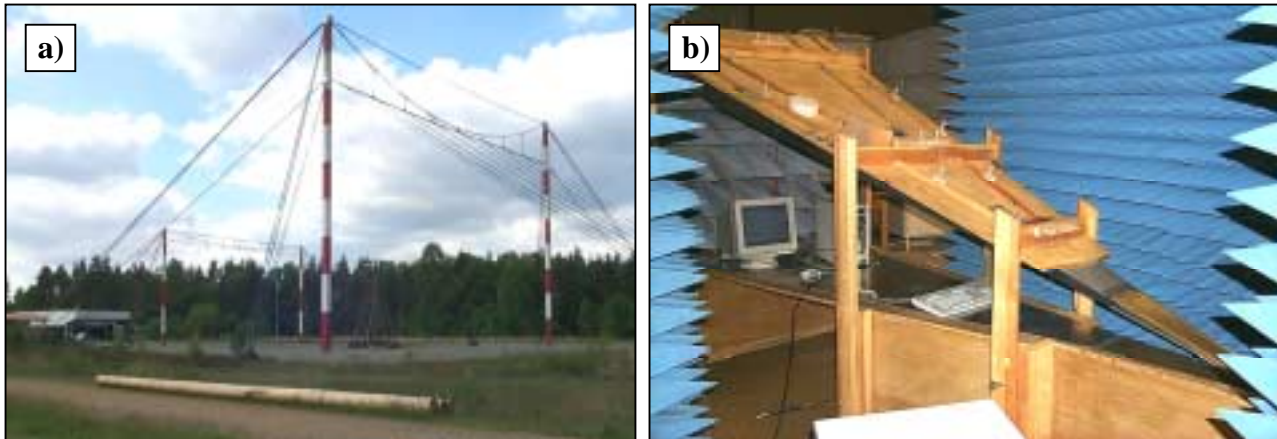


Fig. 2. Waveguides

III. DEFINITIONS

To describe the different failure effects two quantities have been defined [4]. The **B**reakdown **F**ailure **R**ate (**BFR**) has been defined as the number of breakdowns of a system, divided by the number of pulses applied to it (Fig. 3a). A breakdown means no physical damage is done to the system. After a reset (self-, external- or power reset) the system is going back into function. The **D**estruction **F**ailure **R**ate (**DFR**) of the device under test has been defined as the number of destructions divided by the number of pulses applied to the system. Destruction is defined as a physical damage of the system so that the system will not recover without a hardware repair. The **BFR** and **DFR** behaves in principle as shown in Fig. 3b. As important parameters for the description of the susceptibility of a system four quantities were defined. The **B**reakdown **T**hreshold (**BT**) specifies the value of the electrical field strength, at which the **BFR** gets 5% of the maximum value. The **B**reakdown **B**andwidth (**BB**) is defined as the span of the electrical field strength, in which the **BFR** changes from 5% to 95% of the maximum. Äquivalent definitions were done for the destruction failure rate **DFR**.

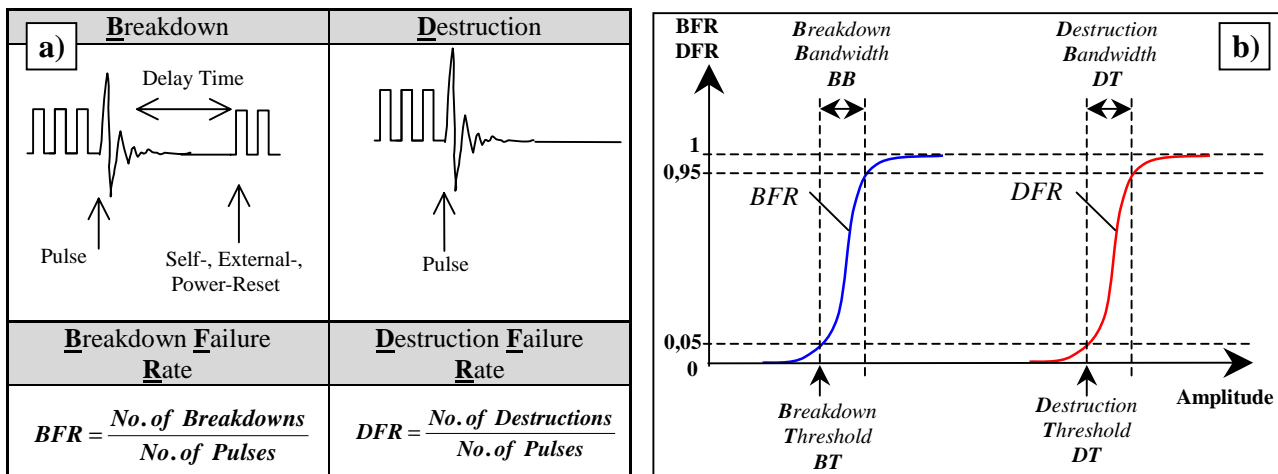


Fig. 3. a) Failure Rates b) BFR, DFR - Principle Behavior and Definitions

IV. SUSCEPTIBILITY OF LOGIC-DEVICES

During the investigations ten different semiconductor technologies (six TTL-, four CMOS-technologies) have been tested (Table 1) concerning the susceptibility to EMP and UWB pulses. NANDs, inverter, generic array logic devices and shift registers were chosen to observe the influence of the technology on the destruction effects.

Table 1. Tested Technologies

TTL-Technology					
Standard	Schottky (S)	Low Power Schottky (LS)	Advanced Schottky (AS)	Advanced Low Power Schottky (ALS)	Fairchild Advanced Schottky (FAST)
CMOS-Technology					
High Speed (HC)	High Speed TTL-compatible (HCT)	Advanced (AC)	Advanced TTL-compatible (ACT)		

IV.1 Test Setup

To apply the different pulses to the EUT a modular setup has been realized (Fig. 4). Ten separate channels were built with a combination of different printed circuit boards. The circuit boards were combined with ribbon cables to realize different coupling lengths at the input and output pins of the devices under test.

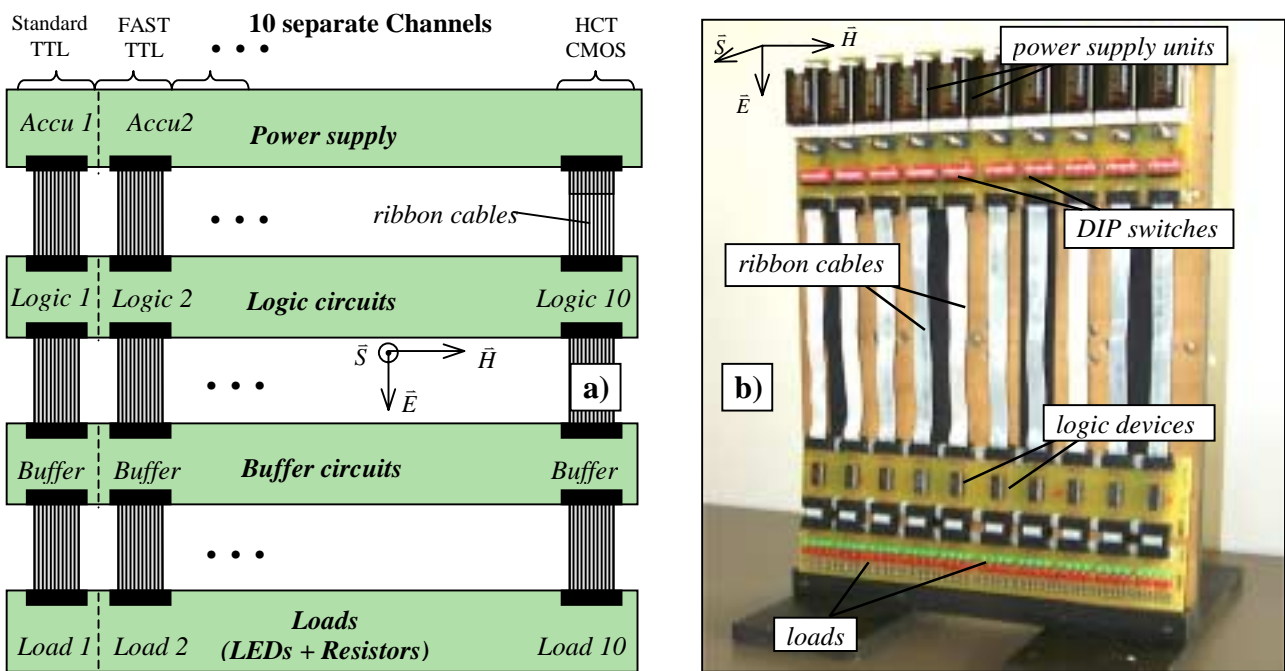


Fig. 4. a) Test Setup - Principle b) NAND Test Setup - Realization

Fig. 4b shows a NAND test setup with 20 cm ribbon cable length at the input pins and ≈ 0 cm ribbon cable length at the output pins of the test devices. The power supply is realized with ten different accumulators. DIP switches were implemented to the power supply unit to adjust arbitrary bit patterns at the input pins. LEDs and resistors were used as loads to observe the operating states of the devices.

IV.2 Measurement Results

As a first result it can be noticed, that CMOS-devices first gets reversible breakdowns which can be reversed by switching the power off and on again. At much higher field amplitudes non reversible destructions occur. This effect can be explained by a parasitic thyristor as a result of the vicinity of complementary n- and p-channel transistors in CMOS devices described in [5]. Fig. 5 shows the BFR and DFR of Inverter-devices built in four different CMOS technologies and six different TTL technologies.

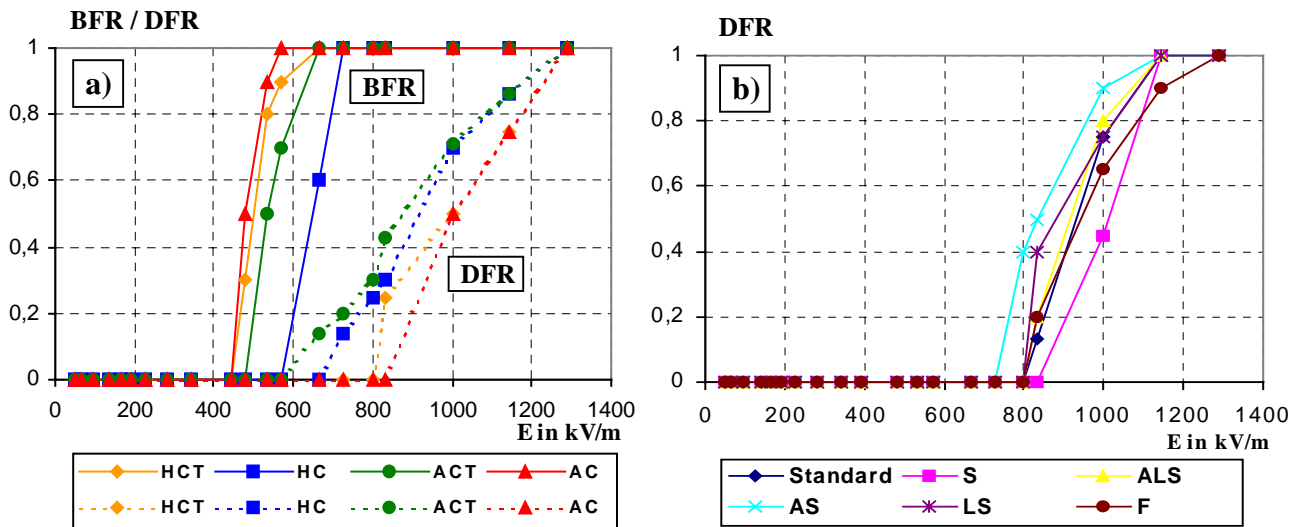


Fig. 5. Breakdown (BFR) and Destruction Failure Rate (DFR) of CMOS (a) and TTL (b) Inverter Devices

The comparison of CMOS- with TTL-Inverter-devices shows, that the destruction thresholds are similar, but that TTL-Inverter-devices only get non reversible destructions and at lower field amplitudes no breakdowns occurred in contrary to the behavior of CMOS-Inverter-devices. The same effects were observed during the investigation of NAND devices. Fig. 6 shows the Breakdown- (BT) and Destruction threshold (DT) of NAND- and Inverter-devices built in ten different technologies (compare Table 1) with 20 cm ribbon cable length at the output pins.

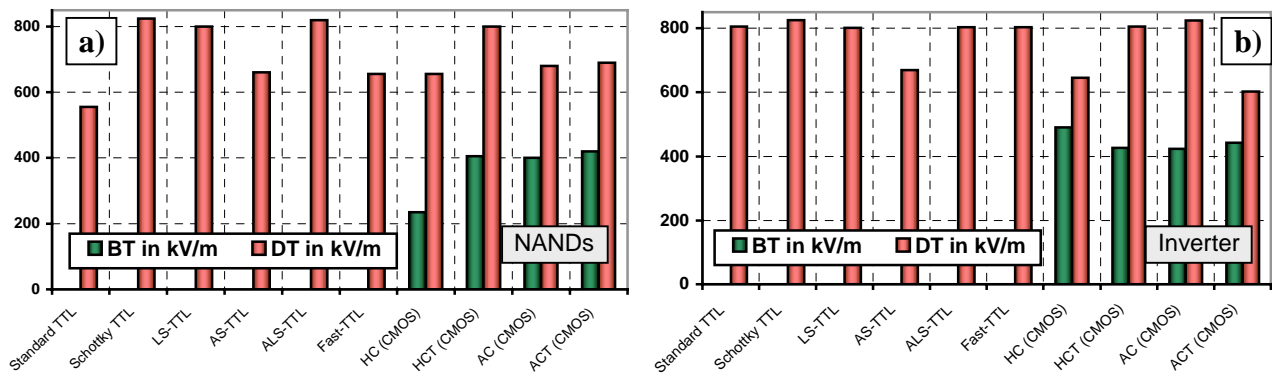


Fig. 6. Breakdown (BT) and Destruction (DT) Threshold of CMOS and TTL Devices a) NANDs b) Inverter

V. SUMMARY

The investigation of the susceptibility of logic devices built in ten different semiconductor technologies to EMP and UWB pulses has shown, that CMOS devices first gets reversible breakdowns and at much higher field amplitudes non reversible destructions occur. The destruction thresholds of TTL and CMOS devices are similar but TTL devices always gets non reversible destructions.

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