Design & Implementation of A Reverse Traffic Channel for CDMA System

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***Abstract*- The main purpose of this project is the design and implementation of a communication system using VLSI technology, to implement it. The system used here is the code division multiple access (CDMA) communication system. The design is focused on the traffic channel of the reverse link. We use Direct Sequence Spread Spectrum technique, which is one of the most common and cost-effective forms of modulation for a spread spectrum system. Direct sequence requires a code sequence to be modulated with the carrier. Any form of modulation can be used. FPGA advantage was used as the design tool on Mentor Graphics EDA tools. The design of the transmitter is implemented on FPGA ALTERA chip (FLEX 10K part no).**

I. Introduction

The market of wireless communication is expected to increase dramatically in the late 1990s and beyond, and this expected high demand has led many service providers to investigate digital technology to satisfy the increasing demand. Spread spectrum has been used for a long time in military communications to resist intentional jamming and to achieve low-probability of detection. However, in recent years,extensive investigations have been carried out into the application of a code division multiple access (CDMA) system in the commercial porpuses.
It appears that CDMA is the strongest candidate for the third-generation wireless personal communication systems. Many research and development (R&D) projects in the field of wideband CDMA have been going on in Europe, Japan, the United States, and Korea.
Emerging requirements for higher rate data services and better spectrum efficiency are the main drivers identified for the third-generation mobile radio systems. Service providers, both cellular and PCS carriers, have deployed commercial CDMA systems in major metropolitan areas. The IS-95 CDMA is now being used in numerous cellular and PCS markets around the world. Service providers are deploying these systems in their markets, where there are mounting demands for higher capacity.
Spread-spectrum is a means of transmission in which the signal occupies a bandwidth in excess of the minimum necessary to send the information; the band spread is accomplished by means of a code that is independent of the data, and a synchronized reception with the code at the receiver issued for dispreading and subsequent data recovery.

II. Background

A. CDMA Concepts

In CDMA, each user is assigned a unique code sequence which is used to encode the information-bearing signal. The receiver, knowing the code sequences of the user, decodes a received signal after reception and recovers the original data. This is possible since the cross-correlations between the code of the desired user and the

codes of the other users are small. Since the bandwidth of the code signal is chosen to be much larger than the bandwidth of the information-bearing signal, the encoding process enlarges (spreads) the spectrum of the signal and is therefore also known as spread-spectrum modulation. The resulting signal is also called a spread-spectrum signal, and CDMA is often denoted as spread-spectrum multiple access (SSMA).
The spectral spreading of the transmitted signal gives to CDMA its multiple access capability. It is therefore important to know the techniques necessary to generate spread-spectrum signals and the properties of these signals. A spread-spectrum modulation technique must be fulfill two criteria: The transmission bandwidth must be much larger than the information bandwidth. The resulting radio-frequency bandwidth is determined by a function other than the information being sent (so the bandwidth is statistically independent of the information signal). This excludes modulation techniques like frequency modulation (FM) and phase modulation (PM).
The ratio of transmitted bandwidth to information bandwidth is called the *processing gain*, G_p, of the spread-spectrum system,

Gp=Bt/Bi

where B_t is the transmission bandwidth and B_i is the bandwidth of the information-bearing signal.
The receiver correlates the received signal with a synchronously generated replica of the spreading code to recover the original information-bearing signal. This implies that the receiver must know the code used to modulate the data.

III. System specifications

* The rate of the output data is 154 times the rate of the input data.
* The CRC (Cyclic Redundancy Check) encoder uses k=4, and n=7; where k is the message length ,and n is the code word length.
* The convolutional encoder uses K=5 ,and R=1/3 ;where K is the constraint length ,and R is the ratio between the input and output code rate.
* The interleaver uses R=11,and C=6; where R is the number of rows,and C is the number of columns.
* The M_ary modulator uses M=8,and K=3 ;where K is the length of grouped symbols ,and M is the length of the generated Walsh word.

The transmitter has been implemented on FPGA chip, ALTERA (FLEX 10K) Part number EPF 10K 10TC 240, with constraint clock frequency 40 MHz.
Whereas, the receiver has been implemented on FPGA chip Xilinx (XC 4000 XL) Part number 4036 XIH 208, with constraint clock frequency 10 MHz.

IV. Design Flow

1- Entering the design using HDL design entry
2- Simulations using the simulation tool (Modelsim), taking into account the test bench for the circuit, to verify the circuit functionality.
3- Synthesis using the synthesis tool (Leonardo), and choose the vendor suitable for the design to calculate the real delay of the circuit.

V. Results

A. TRANSMITTER IMPLEMENTATION

The transmitter is comopsed of four basic blocks (baseband blocks)which are: the cyclic redaundancy check (CRC) encoder, the convolutional encoder, the interleaver, and the modulator.

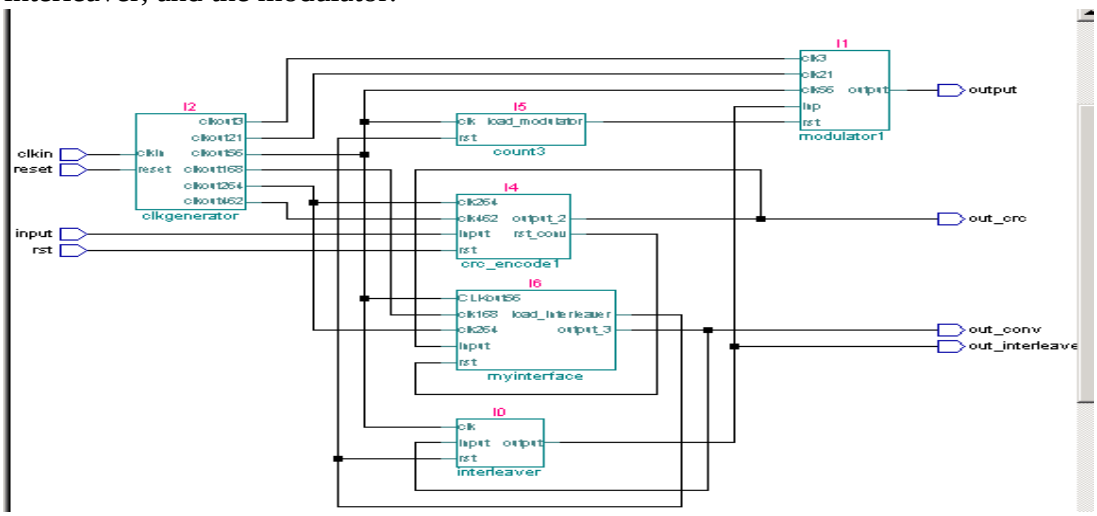

Figure 1. Transmitter block diagram

B. Transmitter after synthesis

The transmitter has been implemented on ALTERA (FLEX10K) part no EPF10K10TC240, with constraint clock frequency 40KHZ.

Figure 2. Transmitter simulation after synthesis

Simulation after synthesis was the same before synthesis with：

```
            Chip/                Input Output Bidir  Memory  Memory
Lcs
POF    Device       Pins  Pins   Pins   Bits % Utilized  LCs  %
Utilized

      Epf10k20rc240-3 4    4      0      0       0  %    719      62 %

User Pins:            4    4      0


Implementation on ALTERA chip

** OUTPUTS **
                                 Fan-In    Fan-Out
Pin      Primitive    Code     INP  FBK  OUT  FBK  Name
142      OUTPUT                 0    1    0    0  out_conv
45       OUTPUT                 0    1    0    0  out_crc
133      OUTPUT                 0    1    0    0  out_interleaver
49       OUTPUT                 0    1    0    0  output
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C. RECEIVER IMPLEMENTATION

The receiver consists of four basic blocks (baseband blocks) which are: the cyclic redundancy check (CRC) decoder, the vitrbi decoder, the deinterleaver, and the demodulator.

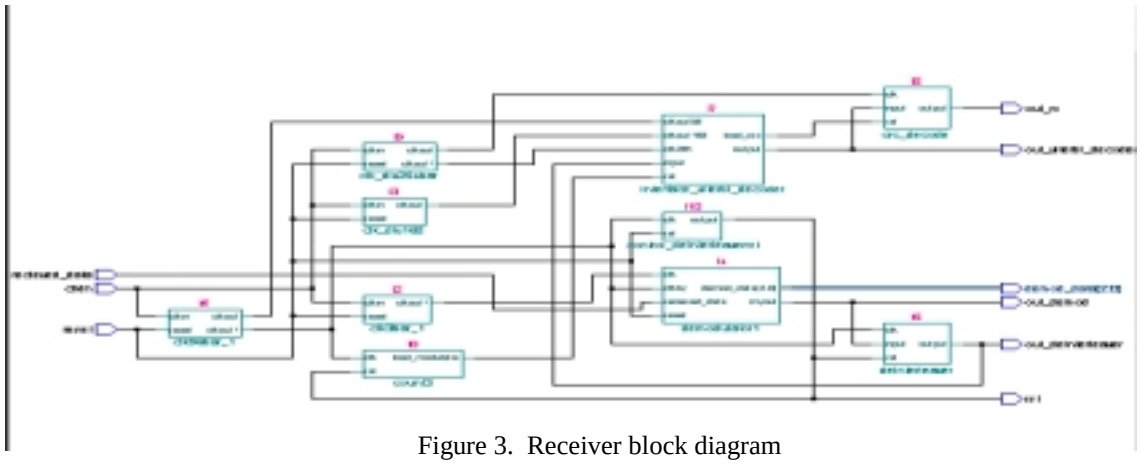

Figure 3. Receiver block diagram

D. Receiver after synthesis

The receiver has been implemented on XLINX(XC4000XL) part no 4036XIHQ208, With constraint clock frequency 40KHZ.

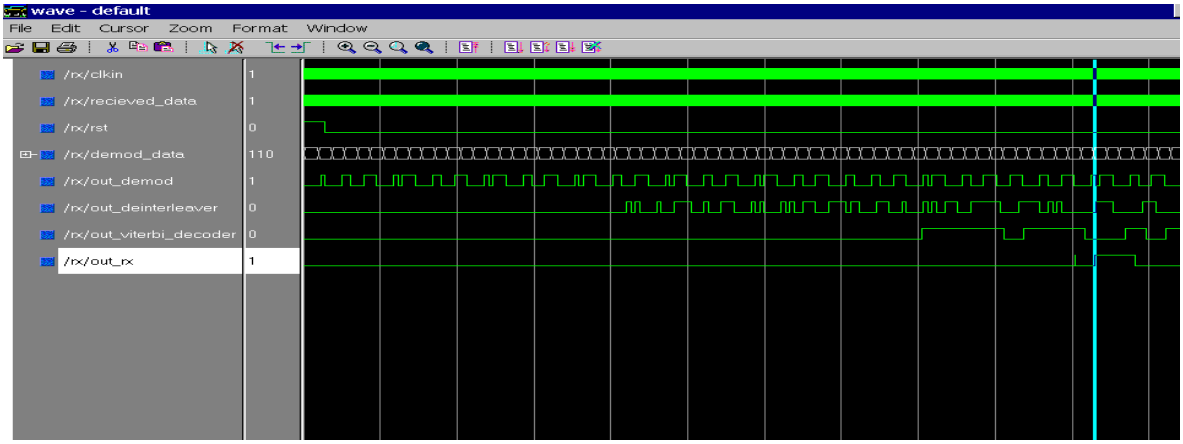

Figure 4. Reciever after synthesis

The receiver after synthesis was identical to before synthesis with design statistics.
Minimum period 58.001 ns (Maximum frequency:17.2 MHZ).
Maximum path delay from the any node:58.001 ns.

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Device Utilization for 4036xlHQ208

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Resource	Used	Avail	Utilization
IOs	11	160	6.88%
FG Function Generators	1110	2592	42.82%
H Function Generators	246	1296	18.98%
CLB Flip Flops	867	2592	33.45%

E. Traffic channel transmitter and receiver (Before synthesis)

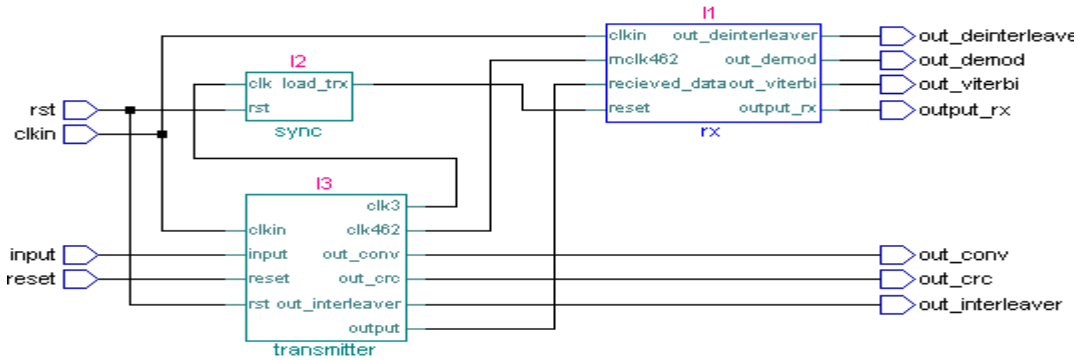

Figure 5. Transceiver block diagram

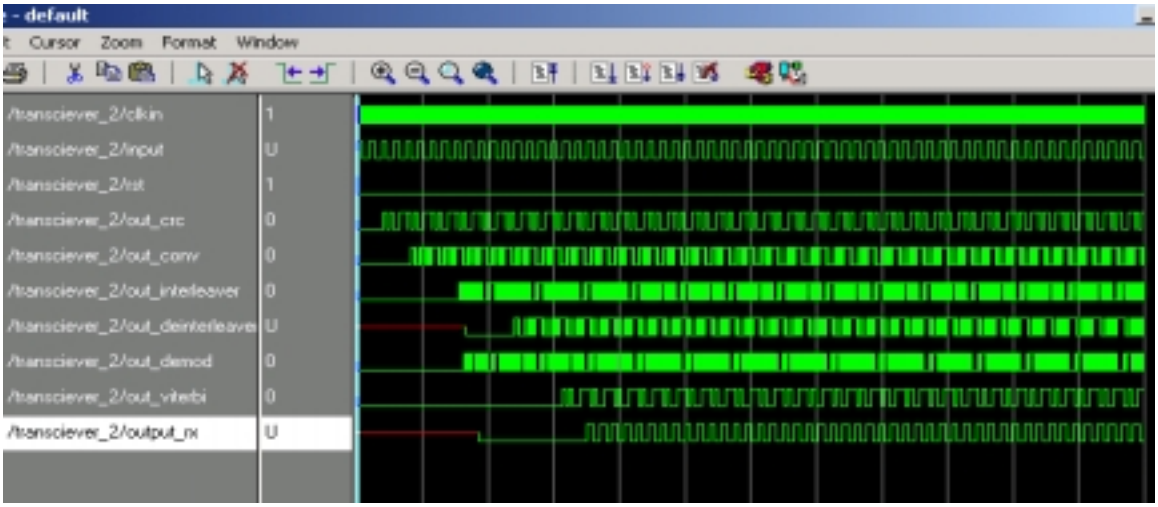

Figure 6. Transmitter and receiver simulation

F. The final FPGA

The final FPGA chip is implemented using Altera (FLEX10K), part no EPF10K10TC240.

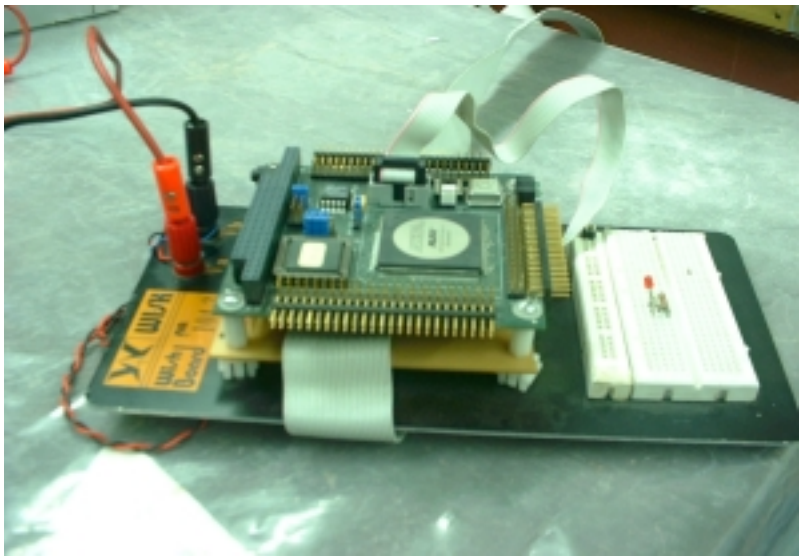

Fig 7. The final FPGA

VI. Conclusion

CDMA is one of the most important multiple access techniques. In this project the reverse traffic channel transmitter and receiver were implemented on FPGA .The after synthesis simulations agreed with before synthesis simulations. The transmitter was connected to the receiver and before synthesis simulation was done to verify the functionality of the transmitter and receiver. We assumed a complete synchronization between the transmitter and the receiver. The channel has been tested using an arbitrary chosen data stream where these data have been transmitted through the implemented transmitter and then received by our implemented receiver. A comparison has been done between the transmitted and received data and satisfactory results have been achieved.

Increasing the number of bits, using the same topology, it is possible to reach the standard rates specified for IS-95 CDMA.

References

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