GMRT CORRELATOR SYSTEM

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ABSTRACT

Giant Metrewave Radio Telescope (GMRT) consists of 30 antennas of 45 meters diameter [1], capable of operating at 6 different frequency bands in the range 50 MHz to 1430 MHz. At any observing band, the analog electronics chain of each antenna produces a signal of 32 MHz bandwidth for each of two orthogonal polarizations. These signals are available as two 16 MHz base-band outputs (upper and lower sidebands of the down-converter) for each polarization. There are thus a total of 120 (30 antennas x 2 side-bands x 2 polarizations, referred as signal channel) analog signal outputs available to the digital back-ends for processing.

INTRODUCTION

The GMRT correlator is an FX type correlator, which runs at 32 MHz. The correlator produces the correlated output between any two signal channels of the same polarizations and same sideband, from two different antennas (two RR and two LL). However, the Multiplier and Accumulator subsystem of GMRT correlator can be reconfigured to give all four Stokes parameters for any one of the two sidebands. The upper and lower sideband signals each consisting of 60 signal (30 antennas x 2 polarizations) are handled by 2 nearly independent correlator systems. The correlator consists of systems and subsystems briefly described in following sections and subsections for giving the required outputs.

GMRT CORRELATOR SYSTEM

The fig 1 shows block diagram of GMRT correlator and other digital back-ends. The correlator produces the correlated output between any two signal channels of the same polarizations and same sideband, from two different antennas. The description in this paper refers to the complete two sideband correlator system.

The Sampler subsystem

The sampler section derives its input from the base-band. The correlator consists of 60 sampler cards. Each card has two signal channels which are fed two orthogonal polarizations. The sampler consists of analog to digital converter (ADC) which samples at the rate of 32 MHz, in accordance with the Nyquist criterion, since the signal from the base-band has bandwidth of 16 MHz. The sampler output is in form of 6-bit data.

The Delay DPC subsystem

Before the signals from the different antennas can be combined in any of the back-ends, they have to be delay corrected to compensate for the different travel time (from a source at infinity) of the radio frequency signals reaching the antennas. Thus each sampler output goes through a digital delay line where the total delay can be adjusted to different values under user control. The Delay DPC system is FPGA (field programmable gate array) based, hence the functions of this system is highly reconfigurable depending on applications and algorithms implemented. Some of the functions currently implemented and possiblities are mentioned below.

- Each card supports four 8 bit input pipelines, in addition there can be 1 more inputs also which can be used for inputting some other information (like input from Omni-directional antenna) also.

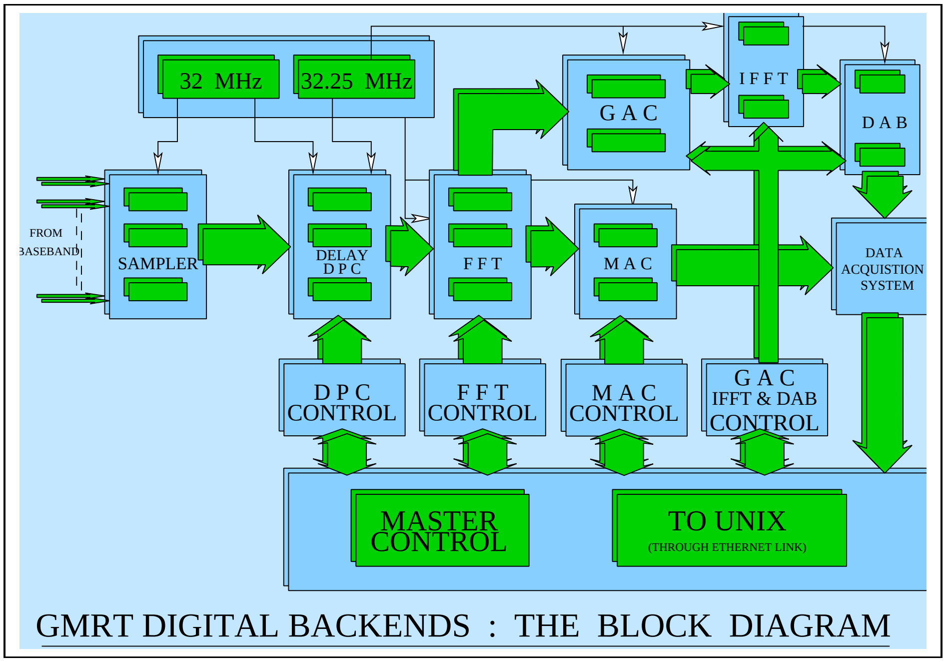

Figure 1: *Block diagram of GMRT correlator and other digital back-ends*

- Data conversion: Conversion of 6 bits of sampler data to 4 bits is done using ROM (Read only memory) as a lookup table and in FPGA. It provides the flexibility in changing input to output mapping.
- Walsh demodulation: Various Walsh sequences can be obtained using a user selectable Walsh word, which depends on the antenna connected to the chain. The start of Walsh sequence is synchronized to a input Walsh sync bit coming from base-band, in addition the start of Walsh sequence can be arbitrarily delayed from sync bit using a Walsh delay word, which is independent from the delay for data.
- Total power readout: The period of total power readout is user selectable and the output is periodically made available and stored in a data buffer from where it can be read by host computer. In addition, the start and stop of accumulation for total power can be synchronized to noise generator on off at the front end, so that the data can be used to determine the system temperature T_{sys} and relative gain variation of each antenna. The total power readout value can be compared with a threshold value decided by more complex algorithms and the result of comparison can be used for flagging data.
- Delaying the signal and Support for De-sampling: Delay of signal is achieved by using a NCO (number controlled oscillator) whose start phase gives the delay of the signal. The output of NCO provides the address of rams where data is stored. The delay values for any signal channel needs to be updated in real-time fashion, as the antennas track a source in the sky. These values are provided well in advance by host computer. The frequency of NCO provides for de-sampling of data (for allowing high spectral resolution modes). Implementation of NCO is done inside FPGA. Delaying the signal (maximum delay of 2.048 milliseconds corresponding to a maximum baseline of about 614 km).
- Channel multiplexing (for enabling polarization modes of the correlator and for diagnostics).
- Data blanking for desired duration on external request or on detection of interference through some suitable algorithm.
- Other functions: Complex filtering can also be done on data and desired band can be selected for output from the incoming data, by using FIR or other digital filtering technique.

There are 30 Delay DPC cards. All four signal channel coming from one antenna goes through same delay card.

The FFT subsystem

The delay corrected signal from each signal channel is then Fourier transformed in real-time. The functions of the FFT (Fast Fourier Transform: Algorithm to perform Digital Fourier Transform) card card shown in fig 3 can be broadly classified (in order they are performed in the card) into the following:

- Fringe stopping: As the earth rotates, each antenna experiences differing radial velocities with respect to the source. Hence, the signal at each antenna is Doppler shifted in frequency by different amounts depending on the position of antenna in the array. This effect is corrected for by multiplying the delay corrected signal by $e^{-j\omega_{fi}t}$, where ω_{fi} is the fringe frequency of i^{th} antenna. A set of ROM (Read Only Memory) chips addressed by $30\ bit$ NCO and digitized $4\ bit$ delay corrected signal channel $s(nT)$ (T is sampling time and n is sample number) is used for this purpose. The output of the fringe ROM is of the form $(a + ib) \times 2^{-c}$ with ($N_r = 7, N_i = 7, N_e = 2$) format (where, N_r: Number of Real bits, N_i: Number of Imaginary bits, N_e: Number of Common exponent bits) and is equal to $s(nT)e^{-j\omega_{fi}t}$.

- Data windowing: At the first stage of the FFT pipeline fringe stopped data is multiplied by desired window function (512 independent sample) having applications in controlling side-lobe level of FFT. Window function is real only with format (4,0,4) and is stored in RAM (Random Access Memory : read, write). The choice of window function depends on user.

- FFT: A 512 point FFT is achieved (once every $\approx 16\mu s$) by using a pipeline of 5 ASICs that can perform Radix-2 and Radix-4 FFT butterfly after suitable twiddling operation at 32 MHz rate. The input signal ($= s(nT)e^{-j\omega_{fi}t}$) is coded into format (7,7,4) used within the FFT mode of the VLBA (Very Large Baseline Array) chip. This gives a continuous stream of 256 complex spectral channels (as 512 point FFT produces 256 complex spectral channels). Figure 3 gives a block diagram showing calculation of FFT in GMRT correlator.

- FSTC: Fractional sampler time corrections (i.e. delay corrections that are fraction of the sampling interval) are achieved by multiplying the complex spectra at the output of the FFT pipeline by the relevant phase gradients. Strictly speaking this is achieved by adding suitable phase (θ_{nFSTC} depending on spectral channel n and phase gradient, which in-turn depend on delay left uncorrected in delay section) to the final stage twiddle phase (θ_{nTWID}) just before the last radix-2 operation. This is shown in fig 3.

Each FFT engine is a completely pipelined system i.e. for every data point that enters into FFT engine, one data point leaves out of system. It expects one number every $31.25ns$, and outputs one complex number in (4,4,4) format (after truncating mantissas) every $31.25ns$. There are in all 60 FFT cards handling 120 outputs from delay cards. These 60 FFT cards are controlled by 12-control cards. The output of two pipelines in one FFT card is time multiplexed and is available for following systems simultaneously through translate (A subsystem to convert incoming TTL data into 4 copies of ECL Data) subsystem.

1. The Multiplier and Accumulator system.

2. Array combiner system : Used mainly for processing pulsar data [2], (not described here).

The MAC subsystem

The Multiplier and Accumulator (MAC) [3] accepts data from the FFT in $(4, 4, 4)$ format. There are 66 MAC cards, each consisting of 16 ASICs arranged in the form of a 4×4 matrix. These 66 MAC cards are capable of handling 30 antenna two polarization two sideband system, producing all possible self and cross-correlations. Each ASIC accepts data effectively from a pair of antennas (or from the same antenna in case of self-correlators), multiplies corresponding spectral points and adds the products in consecutive locations of a 256 word (complex) accumulator. 11 MAC cards are controlled by a control card.

ACKNOWLEDGEMENTS

The author acknowledges the contribution of all members of GMRT correlator team. Some of the members who have worked alongwith author are Prof. C.R.Subramaniam, Prof. Y. Gupta, Prof. A.P. Rao, Dr. A. Roshi, Mr. R. Malik, Mr. V. Tatke, Mr. U.Puranik, Mr. M. Burse, Mr. K. Dahmiwal, Mr. G. Jangam, Mr. I. Bhonde, Mr. I. Halagi, Mr. C. Kanade. The contribution of author is mostly in designing, debuging and implementation of New Delay DPC subsystem, debugging of FFT subsystem and installation of II sideband of GMRT Correlator system at GMRT site.

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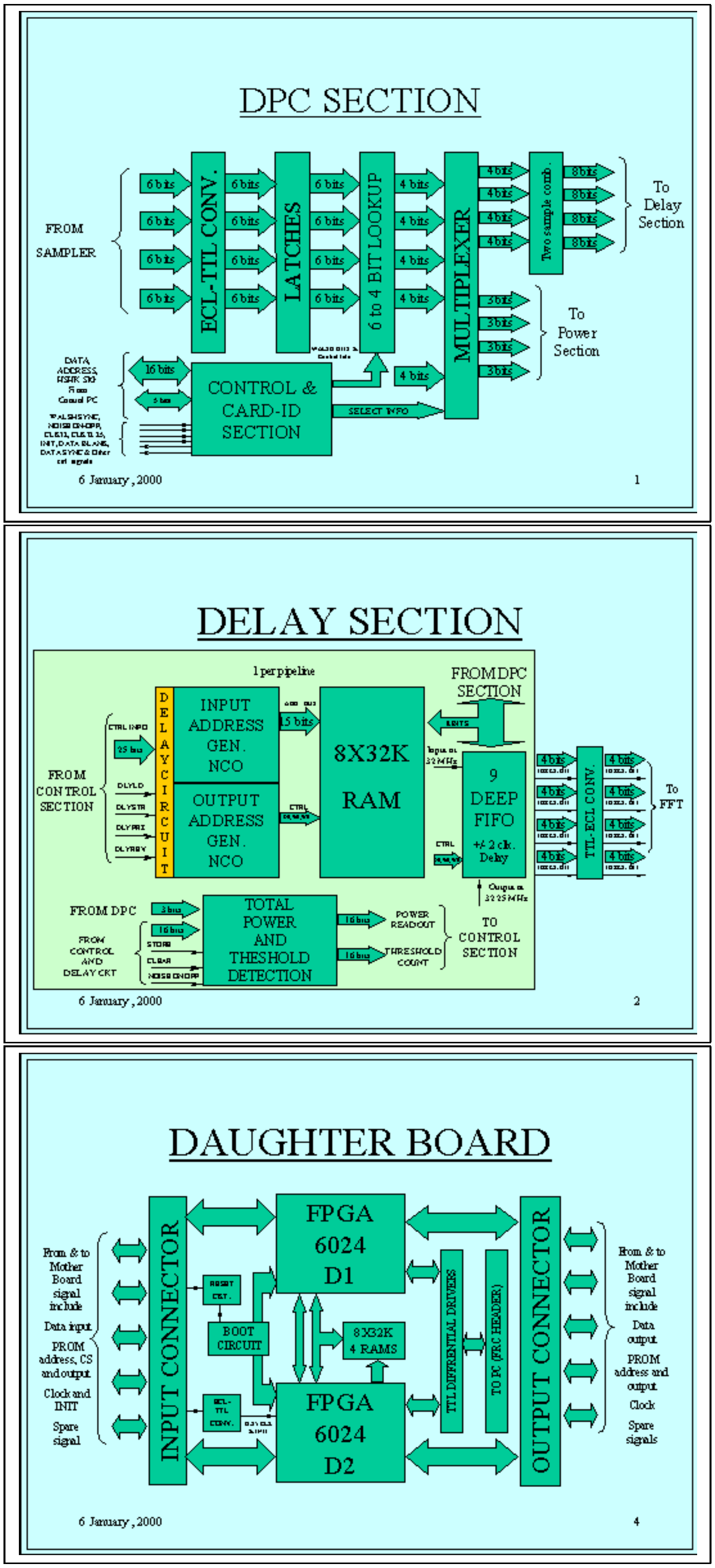

Figure 2: *Block diagram of Delay DPC section*

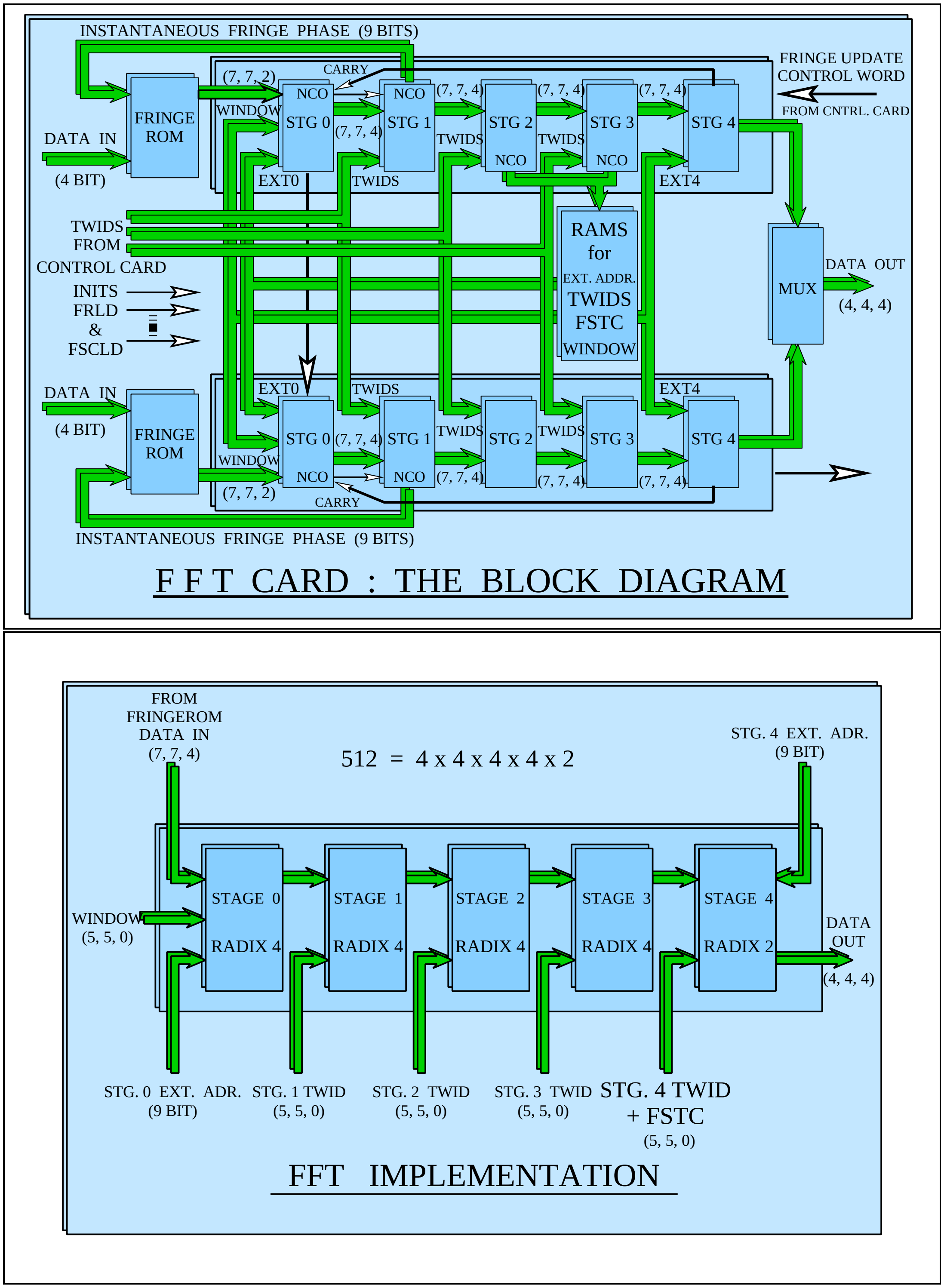

Figure 3: *(a) Block diagram showing FFT card (top) (b) Block diagram showing FFT calculation in FFT card (bottom)*