A NOVEL MICROWAVE EXCITED APPROACH TO ANTENNA EFFECT SIMULATION FOR SUB-0.1μm VLSI DEVICE PROCESS

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ABSTRACT

In this paper we successfully simulate and analyze microwave excited antenna effects for sub-0.1μm VLSI device process. To study the problem, we simulate the structure with the Maxwell equations to compute the induced gate voltage. The Schrödinger-Poisson model is utilized to characterize the electron density quantum degradation. It is found that the process induced antenna effects could largely degrade the characteristics of devices. We find a well-established fabrication processes and optimal VLSI circuit layout parameters may reduce the effects significantly. Consequently, the process and layout optimizations are proposed and done in this work to minimize microwave excited antenna effects.

INTRODUCTION

In recent years, microwave excited plasma has been an alternative and widely used in VLSI processes, such as thin film deposition, defect passivation, and pattern etching. By using this method, the devices characteristics degraded by charge accumulation could be largely reduced. That is, the antenna effect induced from the charge collection during plasma treatment could be neglected [1, 2]. However, in novel integration circuit design, circuit layout becoming more and more complicated; therefore, long metal strips should be needed to provide connection between devices. Consequently, those long metal strips become antennas and collect microwave signal when wafers processed in chambers. L. Trabzon et al [3] has been reported in Fig. 1 that the devices characteristics can be largely degraded during high frequency AC stress. The degradation could saturate at a frequency above 10MHz. This fact indicates that thin gate oxide devices could be largely degraded even only small signals coupling at the gate of MOSFETs during plasma processes. Estimation from Fig. 1 is that, for a 1.3 nm thin gate oxide device, a 1V AC signal could damage the device. To model the effects, we solve the Maxwell's equations and Schrödinger-Poisson (SP) equation to investigate the induced voltage and the charge displacement for the sub-0.1 um device.

A new circuit design is also created and proven to have an efficient improvement. For a series of simulation, we can find that the degradation of this effect could be suppressed when the metal strips longer than 800 um.

EXPERIMENTS

Fig. 2 shows the conventional plasma process chamber. There is a RF generator director connecting to the process chamber with a frequency of 2.45 GHz. This ultra high frequency may couple to circuits on wafers and degrade device characteristics. Fig. 3 is the experimental circuit layout and its cross section views; additionally, it related processes flow is shown in Fig 4. This structure is used in our theoretical calculation. We first solve the Maxwell's equation with a FDTD approach to obtain the induced signal on the gate. The effective voltage is applied as the gate voltage V_G for the SP simulation on a Linux-cluster system [4-7]. The computed charge displacement demonstrates verification for the effect. The amplitude of the test structures is plot as the function of metal length. We can find that while the metal length longer than 800 um, the AC signal will larger than 1.0 V and degrade the fabricated devices. This could cause channel properties and gate oxide reliability reductions.

RESULTS AND DISCUSSIONS

First of all, Fig 1 shows the devices properties degradation under AC stress. This result indicates that the device with a gate oxide of 9.0m could be largely damaged by an AC signal of a amplitude of 8.0 V. As shown in the Fig. 6, we verify the difference of the classical estimation and the quantum mechanical approach. We find there is a significant difference between the Poisson equation and SP model for the 9.0 nm MOSFET at V_G = 8.0. We find the peak value with considering the quantum effects has two times lower than classical approach. The amplitude of the test structures is plot as the function of metal length shown in Fig. 7. Consequently, a MOSFET with a gate oxide of 1.3 nm should be seriously affected by an AC signal of amplitude of 1.0 V. Further comparison could be found in Fig. 8.

Fig. 8 is the simulated charge quantization shift, it can be seen that the gate voltage increased will result in charge peak increased and shift is about 1.0 nm. For low voltage, the charge has slow variation. The effective V_G ~ 1.2 V was computed with the Maxwell equation. In comparison the charge quantization shift of the 9.0 nm silicon dioxide shown in Fig 6, we can found that the charge peak is distributed more away from the Si/SiO2 interface; moreover, the charge distribution is broader. Those facts demonstrate that the devices with thicker gate oxide will get lower correlation about channel interface properties than the thinner one. That is, while the gate oxide becoming thinner and thinner, a slightly changing of channel interface properties will cause devices characteristics seriously degraded. Which is the reason why we insist that a 1volt AC single will affect our thin oxide devices largely.

Fig. 5 introduces a new circuit design for avoiding the antenna effect. Fig. 5a is the device layout and Fig. 5b is the equivalent circuit. By adding those two diodes in the circuit, the coupled AC signal could be largely reduced to only around 0.4V. Consequently, degradation of RF could be nearly neglected. This improvement could be further studied in the simulation results as shown in the insert of Fig. 8.

COLCLUSION

We analyzed microwave excited antenna effects for sub-0.1µm VLSI device process. The Maxwell equations and Schrödinger-Poisson model have been utilized to compute the induced gate voltage and characterize charges density quantum degradation. It has been found that the process induced antenna effects could largely degrade the

characteristics of devices. The proposed process and optimal circuit layout provided an alternative to minimize microwave excited antenna effects.

ACKNOWLEDGEMENTS

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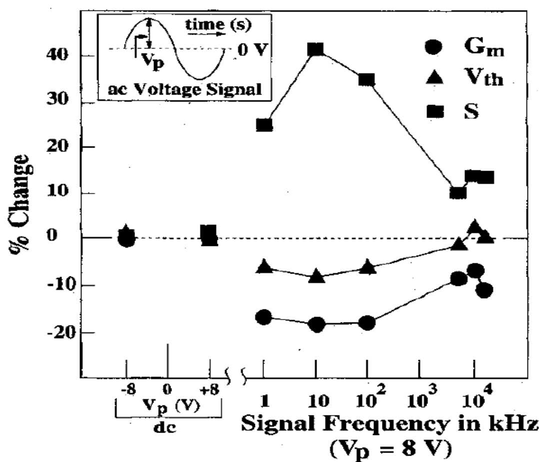

Fig. 1. Device characteristics are largely degraded during high frequency AC stress.

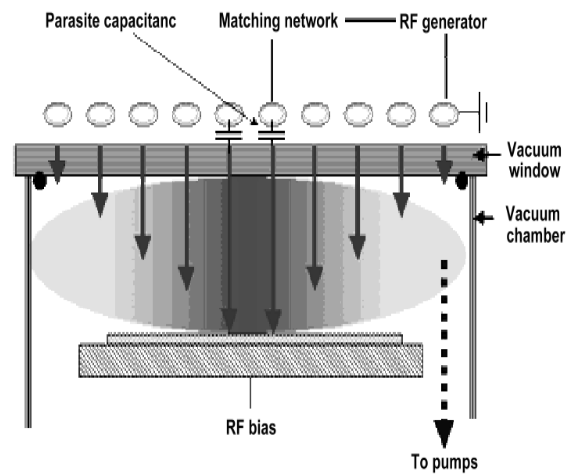

Fig. 2. A conventional plasma process chamber.

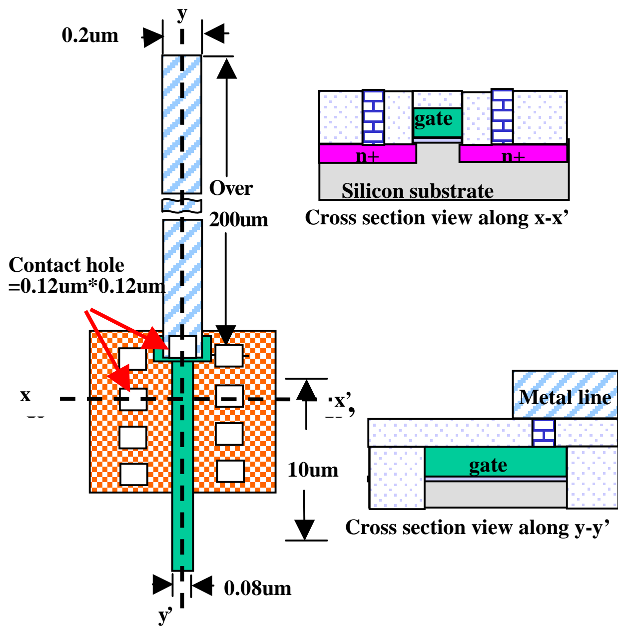

Fig. 3. The circuit layout and its cross section views.

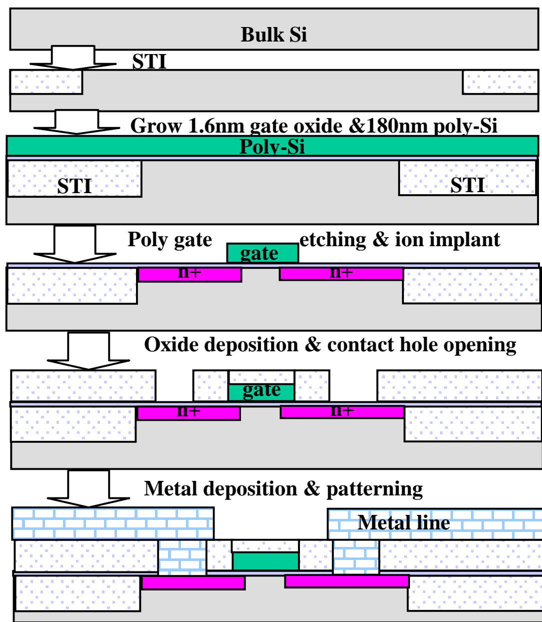

Fig. 4. The processes flow of the device process.

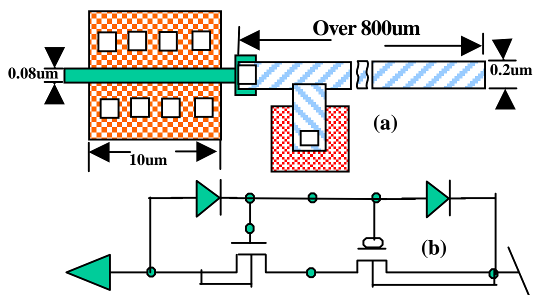

Fig. 5. A proposed circuit for improving the antenna effects.

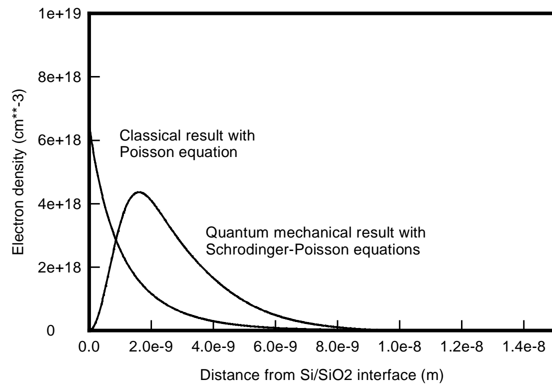

Fig. 6. The charge displacement for Tox = 8 nm device.

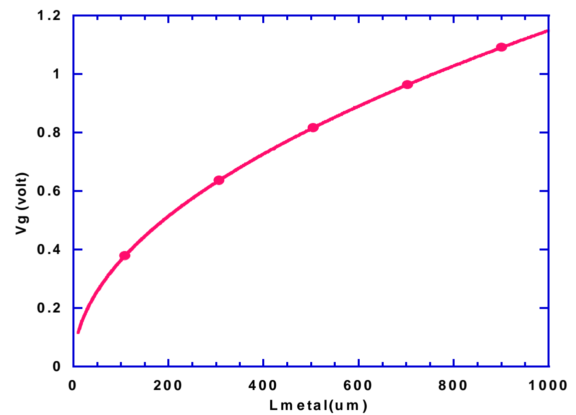

Fig. 7. The amplitude of the test structures versus the metal length.

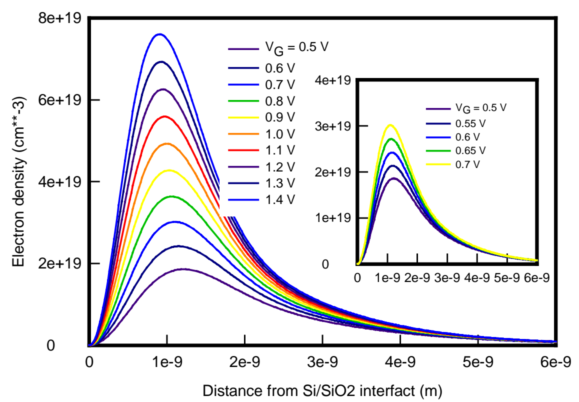

Fig. 8. The charge displacement for different gate voltages. The inserted figure is the charge distribution for the improved structure.