ABSTRACT

This paper presents the design of a CMOS integrated image reject front-end for the application of 950-MHz wireless receivers. It comprises an image reject LNA, and a single-balanced mixer. A second-order active band-pass filter is incorporated into the LNA core to reject the 1.6-GHz image signal. The performance for the receiver front-end circuit designed in a 0.6-μm AMS CMOS technology has a 32 dB conversion gain, 5.4 dB noise figure, -24dBm input IP3, and a maximum of 65 dB image rejection. The total power consumption at 1.5-V supply is 11.7 mW.

INTRODUCTION

Among various receiver architectures, the heterodyne approach has been the most widely accepted for robust operation [1]. The receiver must meet stringent demands for low weight and volume, long battery life, and low cost. To realize this scheme, combining RF ICs with base-band digital signal processing is one of the most attractive solutions. This consequently will demand to eliminate off-chip components such as the SAW image filter, which follows the LNA. A low voltage is also desired to reduce the weight and for corresponding reduction in power consumption in the digital circuitry.

On-chip image rejection could in principle be obtained using image-reject mixer. Typically, these architectures can achieve 30-45 dB of image rejection [2], [3]. An extra 50 dB image rejection should be provided to meet the specification of a heterodyne receiver, that is 80 dB [3]. To address this need, recent research has been focused toward the development of monolithic image rejection schemes using a notch filter centered at the image frequency. A cross-connected differential pair circuit should be used to cancel the losses in the filter. In this paper an approach to implement image rejection function in LNA is described. The proposed active filter is implemented in the signal path of inductively degenerated cascode LNA circuit to reject the image signal utilizing its inherently high Q circuitry. The Q-compensation circuit is not therefore become needed to provide the required image rejection. We demonstrate the designing of such IR-LNA (LNA core + filter) with a single-balanced active mixer to form the integrated image reject front-end receiver.

DESIGN SPECIFICATION

The receiver front-end, Fig. 1, is designed to operate at an RF of 950-MHz and an LO of 1.275-GHz for 325-MHz IF. Hence, the image signal is located at 1.6-GHz. The primary design goal for the image-reject low noise amplifier circuit is to provide a minimum noise figure with the allowed power budget, that is 10 mW. Therefore, a single-ended architecture has been used. A single-balanced active mixer topology is selected. Active mixers achieve conversion gain and require lower LO power than their passive counterparts. A reduced LO drive is a significant advantage in low-voltage IC design.
CIRCUIT DESCRIPTION

Low Noise Amplifier

A tuned amplifier is selected for the LNA core, Fig. 1 in order to minimize the power consumption and to provide additional image rejection. The LNA core consists of three main sections, the transistors $M_1$ and $M_2$, the output LC tuned circuit ($L_p$, $C_p$), and the input LC tuned circuit ($L_g$, $L_s$, and $M_1$'s $C_{gs}$), Fig. 1. The cascode transistor $M_2$ is used to reduce the interaction of the tuned output with the tuned input, and to provide a high reverse isolation, which simplify input port matching. The output LC tuned circuit acts as a high impedance load for the cascode stage at 950-MHz, thus, the gain can be boosted at this frequency. The input tuned circuit is used to optimize the noise performance and achieve the best input match at 950-MHz [4]. $L_s$ is adjusted for maximum power transfer and $M_1$'s $C_{gs}$ for minimum noise figure. The bias current is selected to achieve the power constraint corresponding to the noise figure design goal. The value of $R_2$ is selected to trade-off the input reflection coefficient and the noise figure.

Image-Reject LNA

A second-order active band-pass filter is used to reject the image signal. The filter, Fig. 1, consists of the integrated inductor $L_n$, and transistor $M_n$ with the capacitor source degeneration $C_n$. $L_n$ is selected to be the same as $L_p$ for symmetry (6-nH). The width of $M_n$ is chosen such that the filter has minimum input impedance $Z_{in}$, as seen in (1), at 1.6-GHz.

$$Z_{in} = j\omega L + \frac{1}{j\omega} \left( \frac{1}{C_{gs}} + \frac{1}{C_n} \right) - \frac{g_m}{\omega^2 C_{gs} C_n}$$  \hspace{1cm} (1)

This filter is implemented in the signal path of typical cascode LNA circuit and adjusted the resonance frequency to equal the image frequency. At the image frequency, the impedance $Z_{in}$ looking into the filter is minimum such that all image signal will be extracted from the original path. As a result, the suppression at the image frequency is effectively increased. The negative resistance is used to cancel the losses in the filter, which are mainly due to the low $Q$ of the inductor $L$. $C_n$ with $L_n$ ($g_m$) are adjusted to achieve a deep notch, very high $Q$, at this frequency.

$$Q = \frac{(L/C_n)^{1/2}}{R - (g_m/\omega^2 C_{gs} C_n)}$$  \hspace{1cm} (2)

The power consumption could be decreased while sacrificing the amount of rejection as indicated in (2).

Single-Balanced Mixer

The output of the LNA is downconverted by a single-balanced active mixer to produce the 325-MHz IF signal, Fig. 1. Active mixers with resistive loads enable a high IF frequency for down conversion. It is designed to operate at low-voltage environment. The 0 dBm of LO power driven into each side of the mixing core is a large enough to quickly switch the MOS transistors from their saturation region to their cutoff region and vice versa without overdriving the mixer [5]. Because the mixer core transistors biased near threshold voltage, this allows the mixer to operate with very low voltage supply with the disadvantages of slightly increasing distortion. The source degeneration is realized with a 6-nH integrated inductor, $L_i$. The conversion gain, noise figure, and linearity are optimized by adjusting LO input power, total current, and dc bias points of the LO and RF ports.

SIMULATION PERFORMANCE

The circuit simulations are based on the BSIM3v3 MOS model. A folded wide-channel MOS model [6] is employed, which takes the impact of distributed gate resistance into account, in order to obtain more accurate
simulation results. At 950-MHz, the LNA core has a power gain $S_{21}$ of 13dB with 50Ω output termination. As shown in Fig. 2, the LNA is designed near the optimum noise figure (the minimum value, $NF_{min}$). It has a $NF$ of 1.8dB and consumes 7.1mW of power. The input match $S_{11}$ is found to be -40dB.

The frequency response of the LNA/Filter (IR-LNA) circuit is shown in Fig. 3. The circuit can achieve a maximum image rejection of 65-dB at 1.6-GHz. The tail current $I_{max}$=2.2 mA, is corresponded to maximum allowed consumption.

A careful attention should be given in designing such tail current $I$. If it has an output resistance $R_o$ of 100kΩ, the circuit will achieve a maximum of image rejection 53dB. The image rejection would be degraded down to 37dB if $R_o$=10 kΩ. The IR-LNA NF is 2.4dB and consumes 10.3mW of power.

The IIP3 of the whole system is dominated by the mixer linearity. Fig. 4 shows the results of a two-tone test. The two input signals located at 800-KHz away from each other are applied to the mixer RF port. The IIP3 is −7 dBm. The mixer has a NF of 12 dB and consumes 1.4mW of power. Table 1 shows the summary of the performance of each circuit. The simulated NF and IIP3 for the receiver front-end are 5.4 dB and −24 dBm respectively. It consumes 11.7 mW of power from 1.5-V supply. The voltage gain is 32.7 dB at 950 MHz.

CONCLUSIONS

A low-power, low-voltage, integrated image reject front-end receiver has been proposed and simulated. The circuit proves to be suitable for highly integrated CMOS receivers employing wideband IF architecture. The simulated NF and IIP3 for the receiver front-end are 5.4 dB and −24 dBm, respectively. It consumes 11.7mW of power from 1.5-V supply in the case of 65-dB image rejection.

REFERENCES

Gain: 13 dB
NF: 1.8 dB
$S_{11}$: -40 dB
Power: 7.1 mW

Gain: 10 dB
NF: 2.4 dB
$S_{11}$: -21 dB
IIP3: -10 dBm
Max. IR: 65 dB
Power: 10.3 mW

Gain: 12 dB
IIP3: -7 dBm
Power: 1.4 mW

**Fig. 1.** Receiver front-end circuit diagram

**Fig. 2.** Simulated NF for the LNA core

**Fig. 3.** Frequency response of IR-LNA circuit

**Fig. 4.** Two-tone IP3 simulation

**Table 1.** The performance summary