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Xilinx MPSoC based implementation of Automatic Modulation Classification

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The present times have seen an exponential rise in different technologies that make communication systems more capable & efficient. Every type of communication occupies a distinct frequency band. Amplitude Modulation, Frequency modulation, Digital Modulation schemes etc all have different frequency bands of transmission. Generally, the demodulation of a received RF signal requires prior knowledge about its modulation type, without this knowledge it is very difficult to demodulate the signal to obtain the message signal. Also, to set up a communication network on a particular frequency band the knowledge of spectrum occupancy is indispensable, without which we might corrupt our signal. An efficient system to sense the spectrum in order to figure out the modulation types present is essential. Designing or selecting RF mixers to down-convert a signal to IF relies on prior spectrum knowledge. Recent advancements in Deep Learning algorithms have established themselves as a reliable approach towards the classification problem. A CNN based approach to classify modulation types present in an incoming RF signal stands out as a reliable solution for modulation classification[1].

The present work proposes a CNN based model for modulation classification in the Vitis AI environment using the DeepSig dataset. The dataset has been used to obtain I/Q values for different modulation types at different SNR values. The predictions made by the proposed CNN model gives us an approximation of the modulation type. Initial development involved the model learning to differentiate between many modulation types, gradually the model has been further extended to learn to classify a mixture of modulation types present in the incoming signal. A Xilinx MPSoC was used to process and perform the inference from the model citing the performance in terms of throughput[2]. After the deployment of the model, an ADC with a sufficiently high sampling rate or a Software-Defined Radio may be used to log signal data and this logged data will be passed into the model running on the Xilinx MPSoC for inference[3]. The Vitis AI software from Xilinx converts the model into an .xmodel file and this is used to run inference on the MPSoC unit.

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